

Compal Confidential

Model Name : D4PB1/D5PB1

File Name : TBD

BOM P/N:43

Compal Confidential

D4PB1/D5PB1
M/B Schematics Document

SKL U22/KBL U22 U42 Processor + DDR4

2017-02-22

Rev:1.0

ZZZ
LA-F241P MB REV1
DAA000EV010
DA2@

ZZZ1
LS-D303P FUN/B
DA400299000
DAS@

ZZZ2
LS-D302P USB/B
DA6001HX000
DAS@

ZZZ3
LS-A133P
DA600101010
DAS@

ZZZ4
LS-D301P LID/B
DA400272000
DAS@

ZZZ5
LS-B734P
DA6001B8010
DAS@

ZZZ5
HDMI LOGO
RC0000003HM
HDMI@

ZZZ
LS-B732P
DA4001YF010
DAS@

ZZZ
DAZ PCB
DAZ11B00100
DAZ@

ZZZ
SMT EMC EE AF241 D4PB1
X4E@EMC
X4EA99BOL01

UC1
FJ8067702739739 SR342 H0 2.5G
CPU_SR342@
SA0000A37N0

UC1
S IC FJ8067702739740 SR341 H0 2.7G ABO
CPU_SR341@
SA0000A34L0

UC1
S IC FJ8067703281813 QN5C Y0 1.8G
CPU_QN5C@
SA0000AQZ10

UC1
S IC FJ8067702739738 SR343 H0 2.4G ABO
CPU_SR343@
SA0000A38M0

UC1
S IC FJ8067702739738 SR22W H0 2.4G ABO
CPU_3860@
SA0000A3860

UC1
S IC FJ8067702739738 QLDP H0 2.4G BGA
CPU_3820@
SA0000A3820

UC1
S IC FJ8067702739739 SR22U H0 2.5G ABO
CPU_3760@
SA0000A3760

UC1
S IC FJ8067702739739 QLDM H0 2.5G BGA
CPU_3720@
SA0000A3720

UC1
S IC FJ8066201924931 SR2F0 D1 2.4G ABO
CPU_2T80@
SA000092T80

UC1
S IC FJ8067702739741 QLDU H0 2.6G BGA
CPU_3L20@
SA0000A3L20

UC1
S IC FJ8067702739740 SR22V H0 2.7G ABO
CPU_3450@
SA0000A3450

UC1
S IC FJ8067702739633 QLYF H0 2.6G BGA
CPU_DO10@
SA0000ADO10

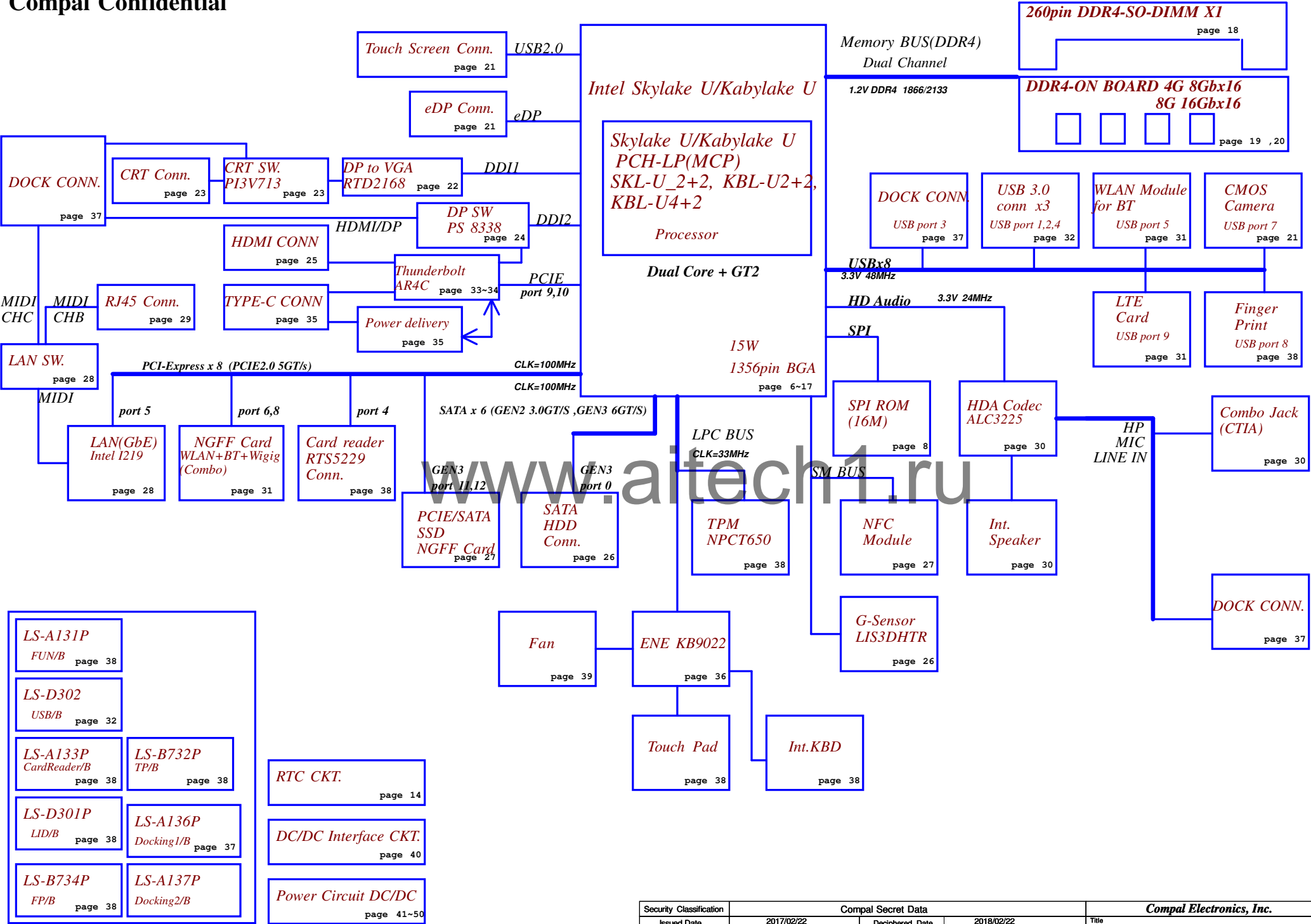
UC1
S IC FJ8067702739628 QLYF H0 2.8G BGA
CPU_DP10@
SA0000ADP10

KBL-R U42



S IC FJ8067703281813 QN5C Y0 1.8G
CPU_QN5C@
SA0000AQZ10

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				Date:	Wednesday, June 14, 2017
				Sheet	1 of 54
				Rev	0.1



Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{BD} min	V _{BD} typ	V _{BD} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

BOM Structure Table

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	dGPU	VGA@
Connector	CONN@	ON Board DDR4	X76OBRAM@
EMC requirement	EMC@	N16S-GT	SGT@
EMC requirement unpop	@EMC@	Without WiGi Funct i on	NOWG@
EMI requirement	@EMI@/EMI@	HDD Redriver	X76TI@/X76PAR@
Thunderbolt Funct i on	TBT@	N16V-GM	VGM@
RF requirement	@RF@/RF@	VRAM BOM Select	X76@
LTE Funct i on	3G@	Single/Dual Rank	SR@/DR@ DR@ is not been used in this project)
UMA only	UMA@		
VPRO Funct i on	VPRO@/NOVPRO@	PD Funct i on	PD@
VGA EMI Requirement	@VGA_EMI@/VGA_EMI@	CPU Code	QH7Y@
VGA UNPOP	@VGA@	ESD requirement	ESD@
VGA RF Requirement	@RF@_VGA@	Touch screen reserve	TS@
VGA Power	22@/23E@	KBL-R U42	U42@
GC6 Funct i on	GC6@/NOGC6@/NGC6	KBL U22	U22@
INTEL CMC	CMC@		
ESPI	ESPI @		

I2C Address Table

BUS	Device	8Bit Read/Write
SOC SMBCLK_1 +3VS	JDIMM1	A4/A5
SOC SMBCLK_1 +3VS	Gsensor U26	30/31
SOC SML0CLK_ +3VS	JNFC1	52/53
SOC SML0CLK_ +3V_LAN	LAN UL1	C8/C9
SOC SML1CLK_1 +3VSDGPU_MAIN	UGPU1	9E/9F
SOC SML1CLK_1 +3VS	Thermal Sensor UU24	98/99
SOC SML1CLK_1 +3VS	PCH_LP	90/91
EC SMB_CK1_ +3VLP_EC	PD U5007	70/71
EC SMB_CK1_ +3VLP_EC	Battery PJP201	16/17
EC SMB_CK1_ +3VLP_EC	Charger PU301	12/13

43 level BOM table

43 Level	Description	BOM Structure
431A0NBOL01	SMT MB AD301 B4DBG QJFC 2.3G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL02	SMT MB AD301 B4DBG QJ8M 2.4G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL03	SMT MB AD301 B4DBG QJKP 2.3G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@
431A0NBOL04	SMT MB AD301 B4DBG QJKK 2.5G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	Res	Vbrd	PCB version	Project	Note
EVT	0K	0v	0.1	New P6	
PVT	12k	0.345V	0.2		
PreMP	15k	0.430V	1		

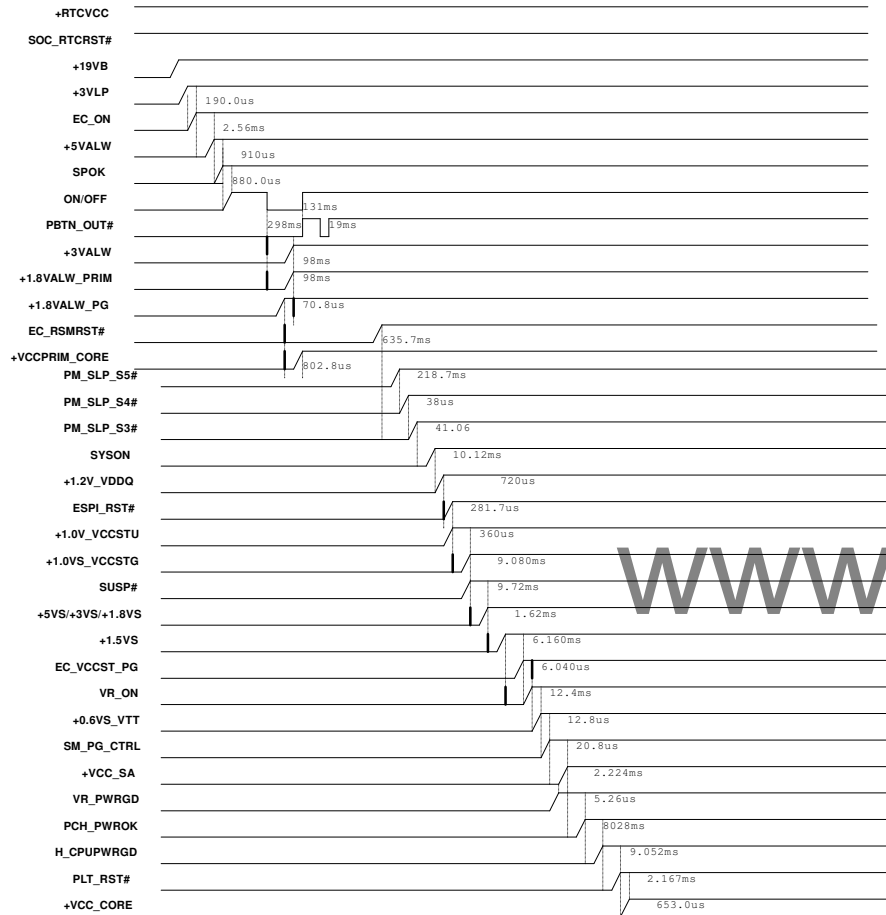
Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON	OFF	OFF
+2.5V	DDR4 +2.5V Power Rail	ON	ON	OFF

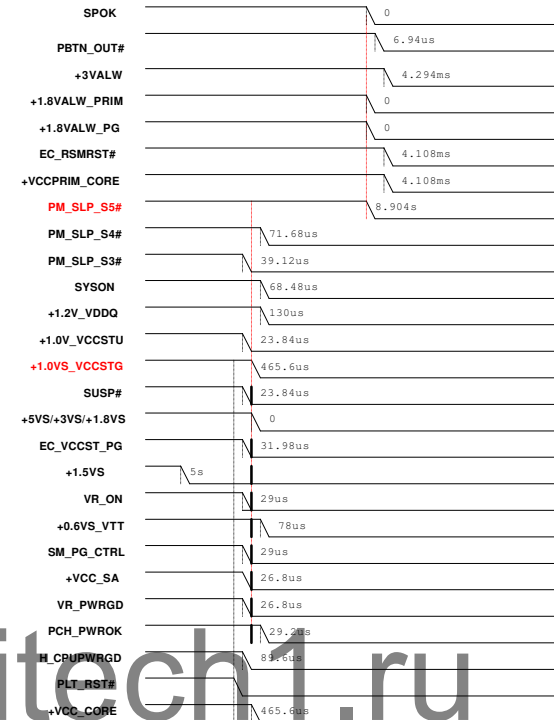
Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

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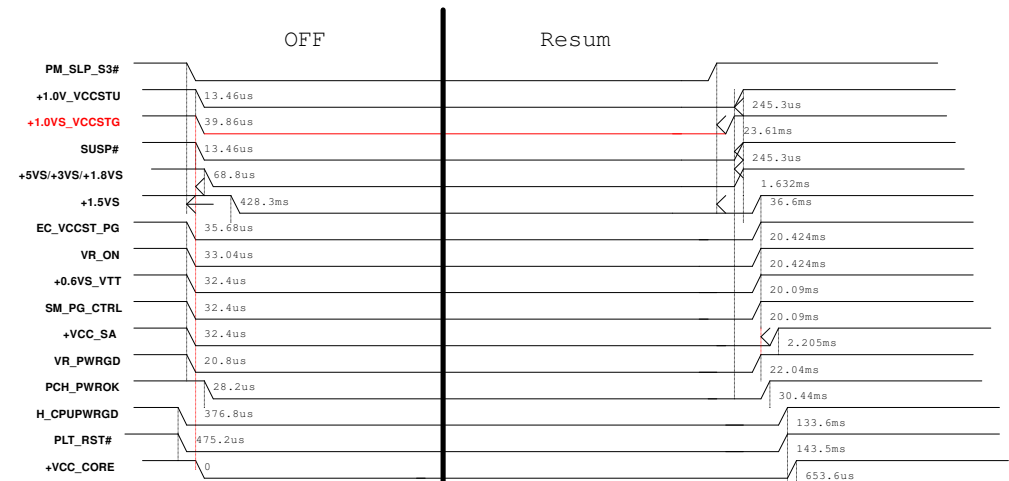
C4PB1/C5PB1 Power on sequence



C4PB1/C5PB1 Power OFF sequence



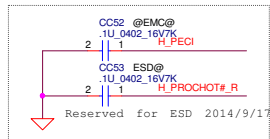
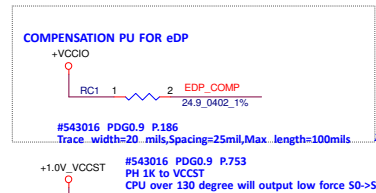
C4PB1/C5PB1 S3 sequence



Functional Strap Definitions

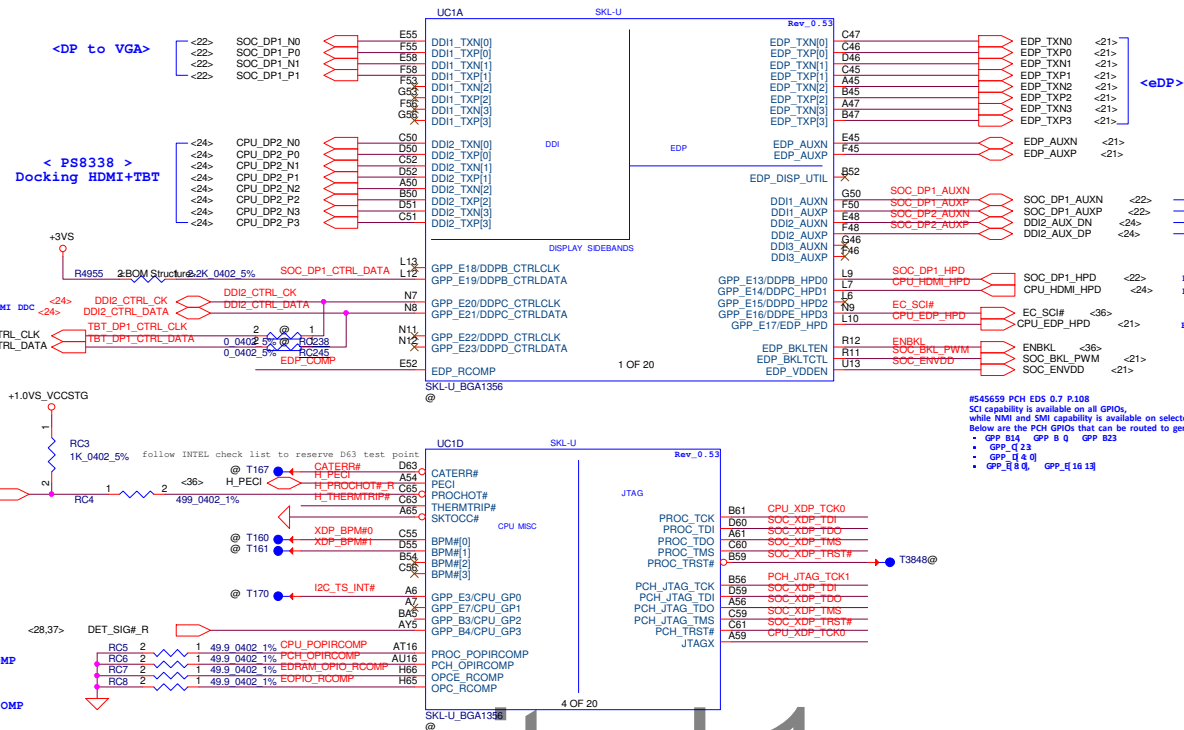
#543016 PDG0.9 P.775

DDPB_CTRLDATA GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA GPP_E23 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 = Port is not detected.
1 = Port is detected.

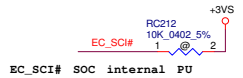


PDG0.9 P.771
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB RVP7 1.0
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD50ohm

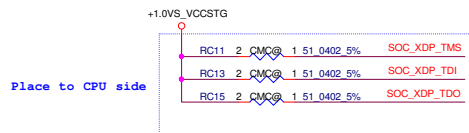


DP Aux (Port B for VGA)
PS8338

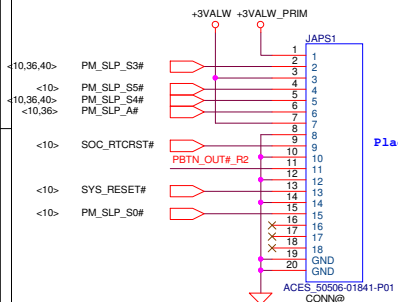


Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
58	GND	GND	NA		60	GND	GND	NA	
Notes: 1. These signals are optional, can be left as CPU/IO/No-Connect. 2. See CPU/IO/No-Connect section for additional routing guidelines. 3. Routing if this signal to CPU/IO is optional.									
9	OSDATA_A1	CPUC1	I/O	Baymax	10	OSDATA_A1	CPUC1	I/O	Baymax
11	OSDATA_A1	CPUC1	I/O	Baymax	12	OSDATA_A1	CPUC1	I/O	Baymax
13	GND	GND	NA		14	GND	GND	NA	
15	OSDATA_A1	CPUC1	I/O	Baymax	16	OSDATA_A1	CPUC1	I/O	Baymax
17	OSDATA_A1	CPUC1	I/O	Baymax	18	OSDATA_A1	CPUC1	I/O	Baymax
19	GND	GND	NA		20	GND	GND	NA	
21	GND	GND	NA		22	GND	GND	NA	
23	OSDATA_B1	CPUC1	I/O	Baymax	24	OSDATA_B1	CPUC1	I/O	Baymax
25	GND	GND	NA		26	GND	GND	NA	
27	OSDATA_B1	CPUC1	I/O	Baymax	28	OSDATA_B1	CPUC1	I/O	Baymax
29	OSDATA_B1	CPUC1	I/O	Baymax	30	OSDATA_B1	CPUC1	I/O	Baymax
31	GND	GND	NA		32	GND	GND	NA	
33	OSDATA_B1	CPUC1	I/O	Baymax	34	OSDATA_B1	CPUC1	I/O	Baymax
35	OSDATA_B1	CPUC1	I/O	Baymax	36	OSDATA_B1	CPUC1	I/O	Baymax
37	GND	GND	NA		38	GND	GND	NA	
39	GND	GND	NA		40	GND	GND	NA	
41	OSDATA_C1	CPUC1	I/O	Baymax	42	OSDATA_C1	CPUC1	I/O	Baymax
43	OSDATA_C1	CPUC1	I/O	Baymax	44	OSDATA_C1	CPUC1	I/O	Baymax
45	OSDATA_C1	CPUC1	I/O	Baymax	46	OSDATA_C1	CPUC1	I/O	Baymax
47	OSDATA_C1	CPUC1	I/O	Baymax	48	OSDATA_C1	CPUC1	I/O	Baymax
49	GND	GND	NA		50	GND	GND	NA	
51	OSDATA_D1	CPUC1	I/O	Baymax	52	OSDATA_D1	CPUC1	I/O	Baymax
53	OSDATA_D1	CPUC1	I/O	Baymax	54	OSDATA_D1	CPUC1	I/O	Baymax
55	OSDATA_D1	CPUC1	I/O	Baymax	56	OSDATA_D1	CPUC1	I/O	Baymax
57	OSDATA_D1	CPUC1	I/O	Baymax	58	OSDATA_D1	CPUC1	I/O	Baymax
59	OSDATA_D1	CPUC1	I/O	Baymax	60	OSDATA_D1	CPUC1	I/O	Baymax

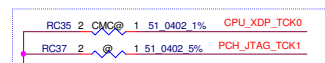
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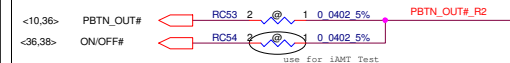
APS CONN



Place to CPU side

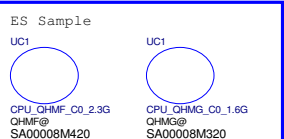
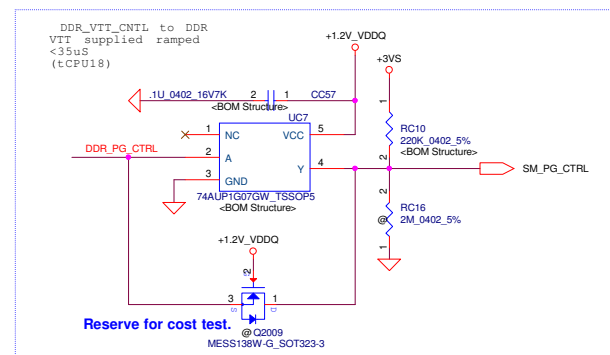
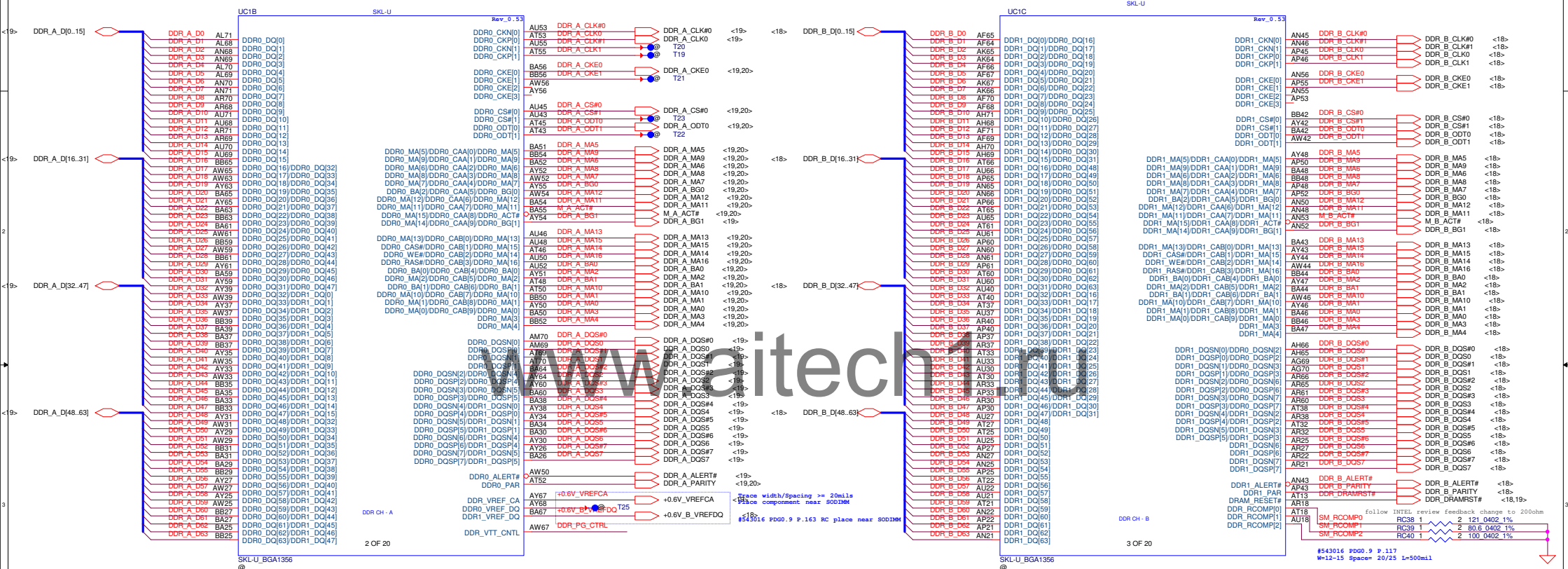


Follow 544924_SkyLake_EDS_Vol_1_Rev_0.93



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Interleaved Memory



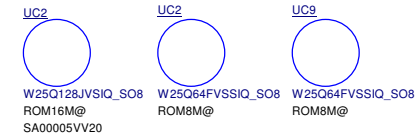
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AR GPIO

WLAN

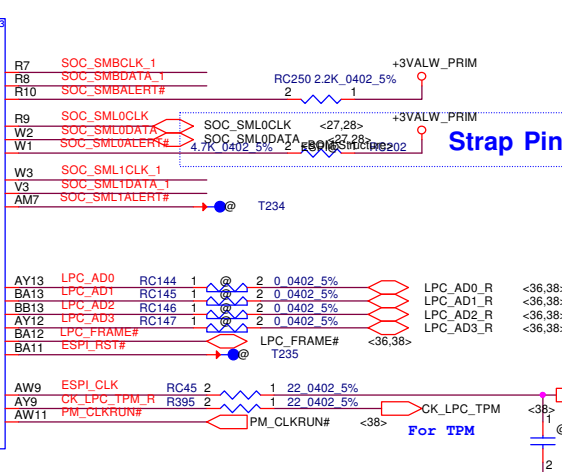
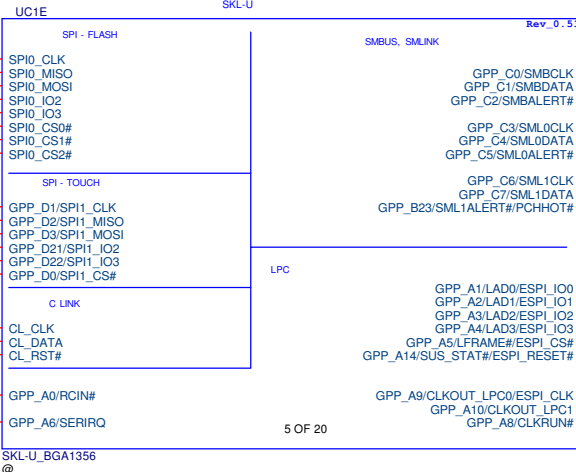
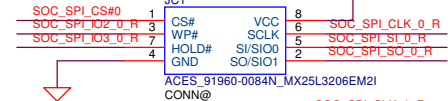
SPI ROM

Single SPI ROM_CS0#



SPI ROM (8MByte)

ROM Socket



SMB

(Link to DDR, G-sensor)

SML0

(Link to NFC, LAN)

SML1

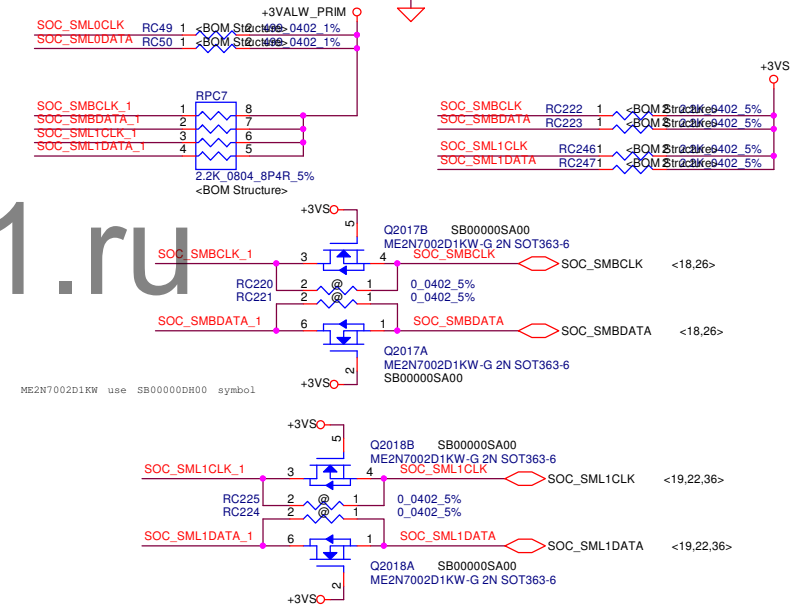
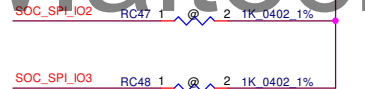
(Link to EC, DGPU, DDR thermal, RTD168)

ESPI / LPC Bus

ESPI : +1.8V
LPC : +3.3V

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2015MOW06 no need PULK on SPI IO2/IO3



SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

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				SKL-U(3/12)SPI,ESPI,SMB,LPC				
				Size	Document Number		Rev	
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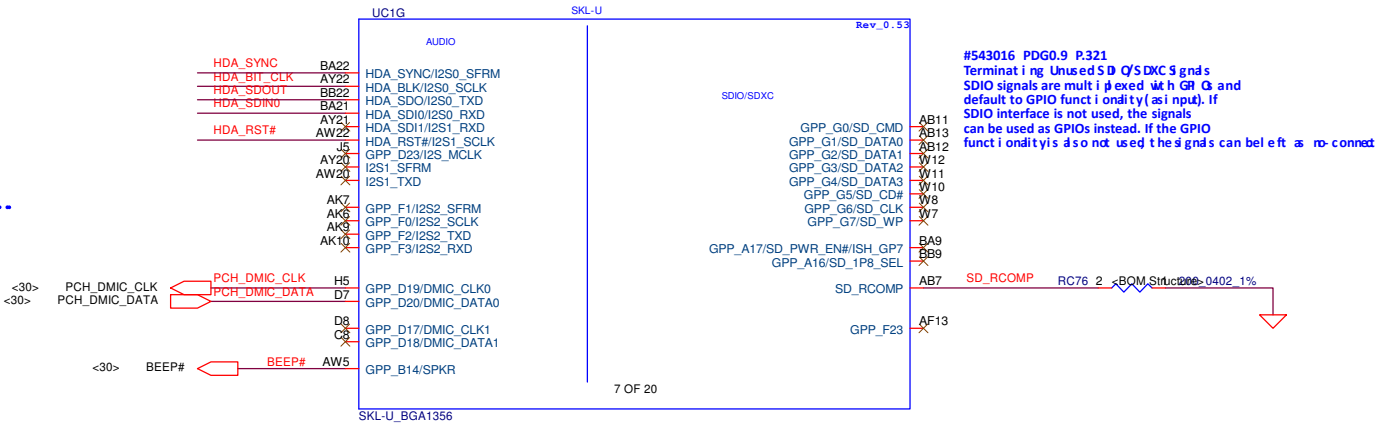
11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
 - SDO double pumped up to 48 Mb/s
 - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)

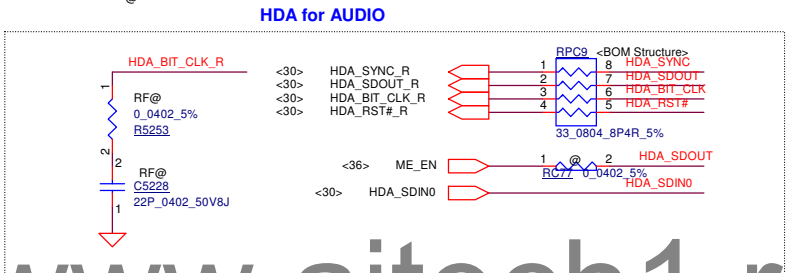
TOP Swap Override
0 = Disable TOP Swap mode.----> AAX05 Use
1 = Enable TOP Swap Mode.



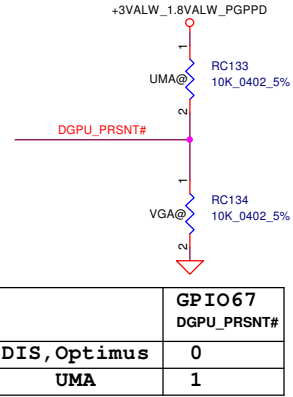
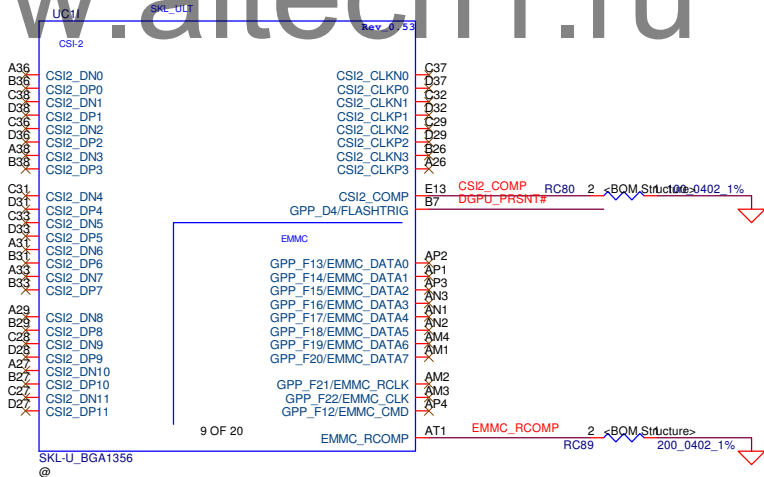
62.3.38 RCOMP Checklist

Table 62-48. RCOMP Checklist

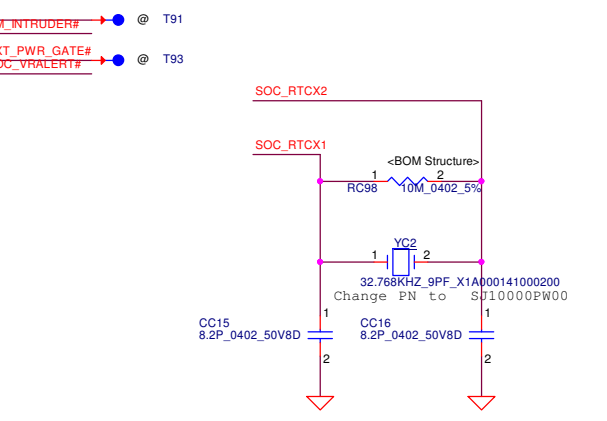
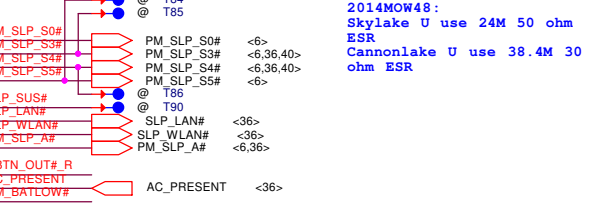
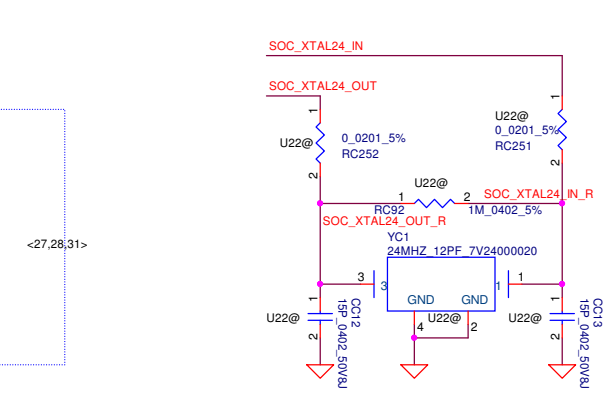
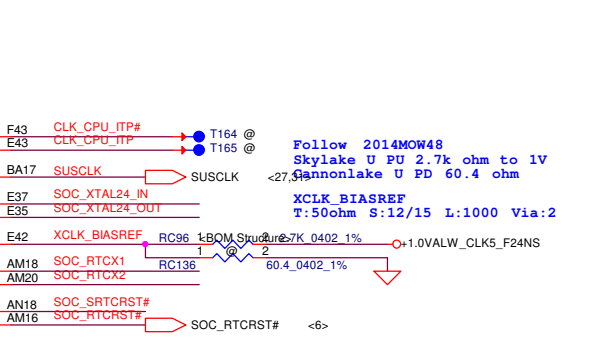
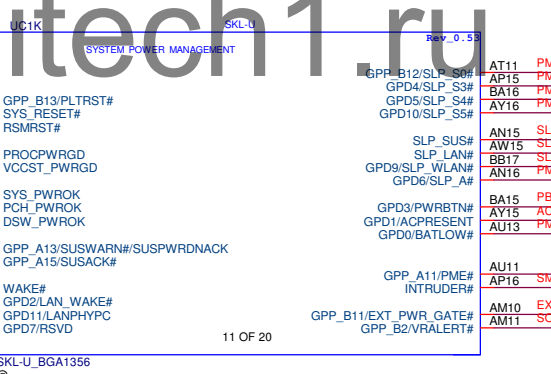
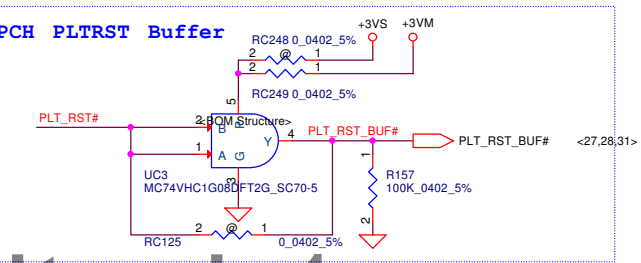
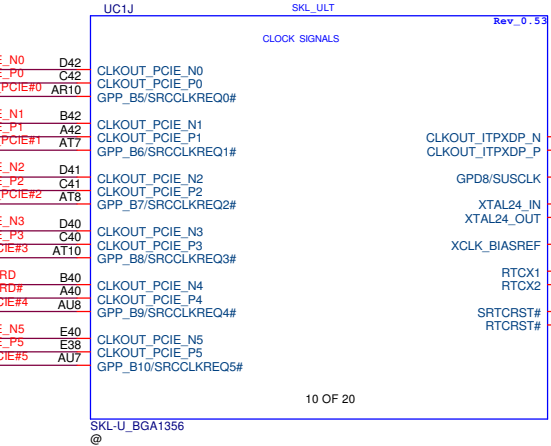
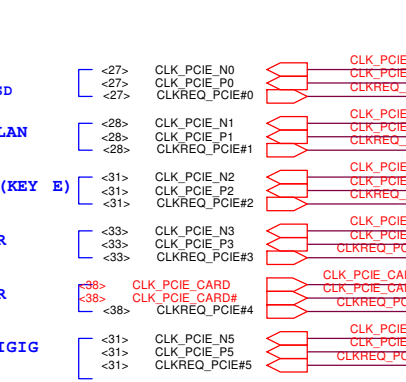
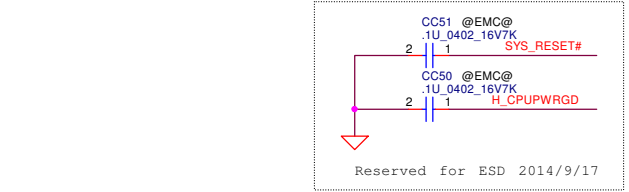
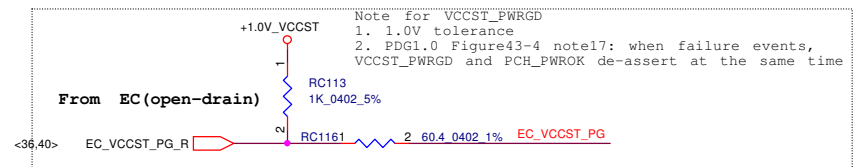
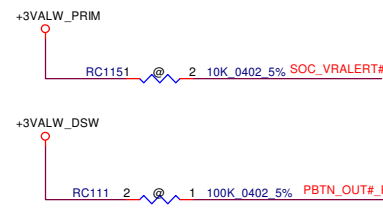
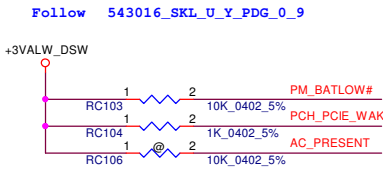
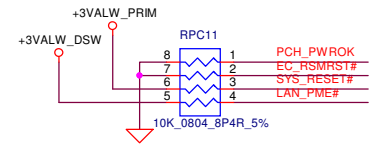
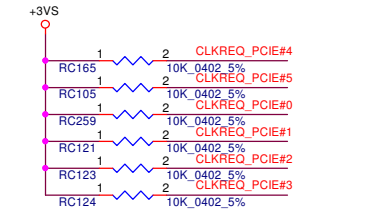
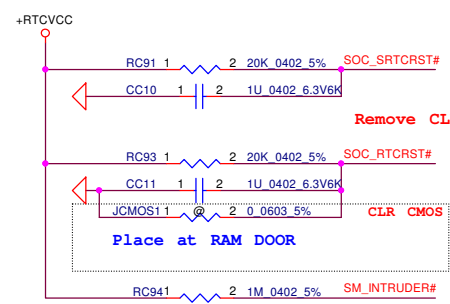
Component	Value	✓
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
PEG_RCOMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND.	
EHMC_RCOMP	200ohms termination to GND.	
PCIE_RCOMP/N	100 ohm +/- 1%. Differential between RCOMP/RCOMP	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	
SD_RCOMP	200ohms termination to GND.	
EHMC_RCOMP	200ohms termination to GND.	
PCH_POPIRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMP/N	100 ohm +/- 1%. Differential between RCOMP/RCOMP	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	



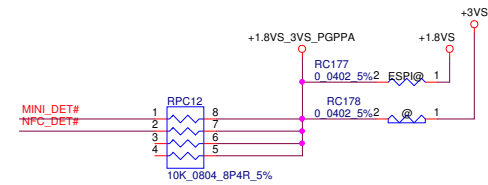
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	GPIO67 DGPU_PRNST#
DIS, Optimus	0
UMA	1

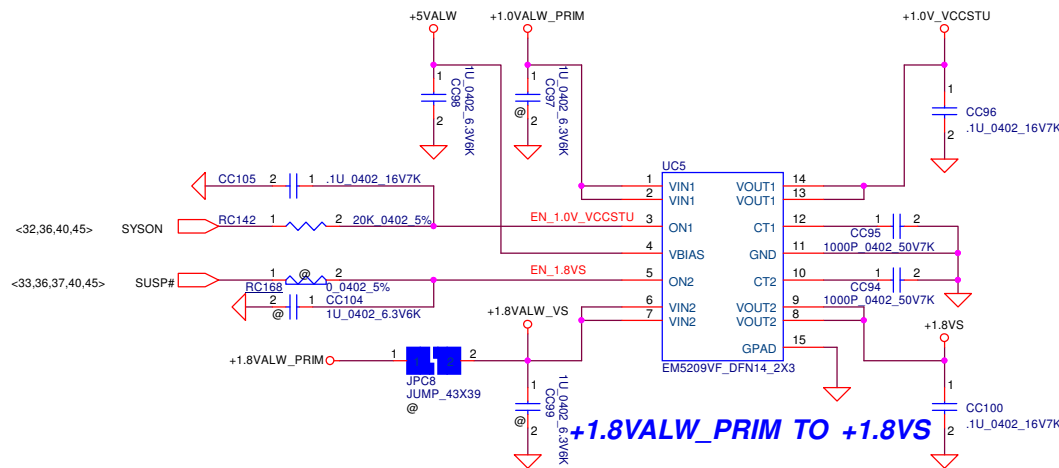


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					Custom	LA-F241P			0.1		
					Date:	Friday, June 09, 2017		Sheet	10	of	54



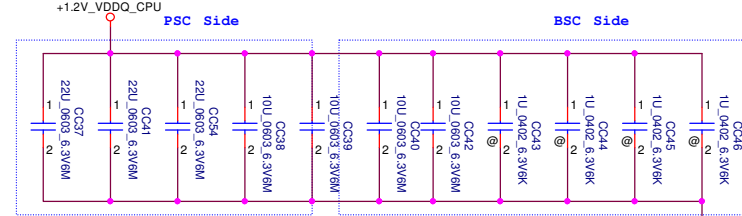
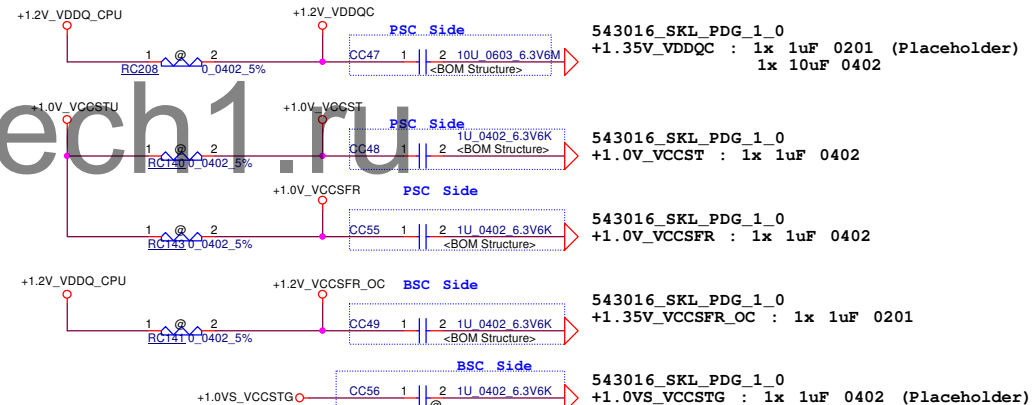
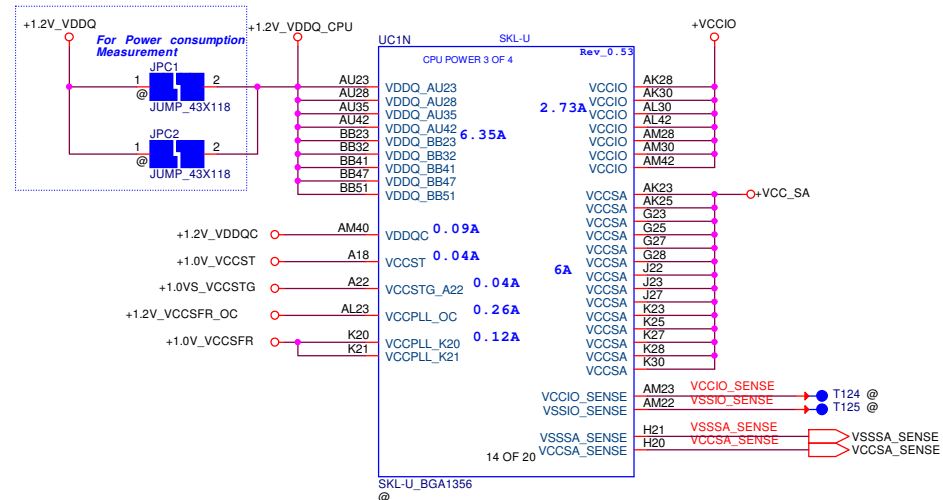
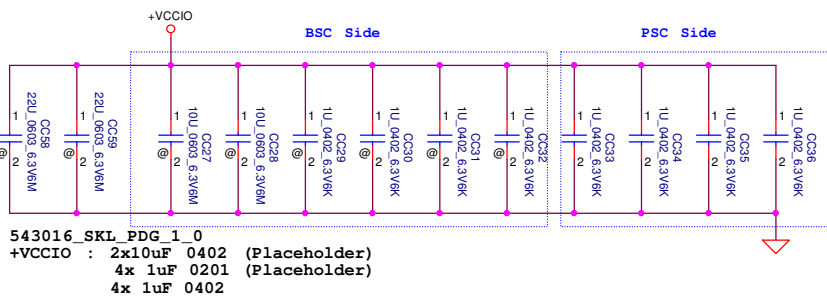
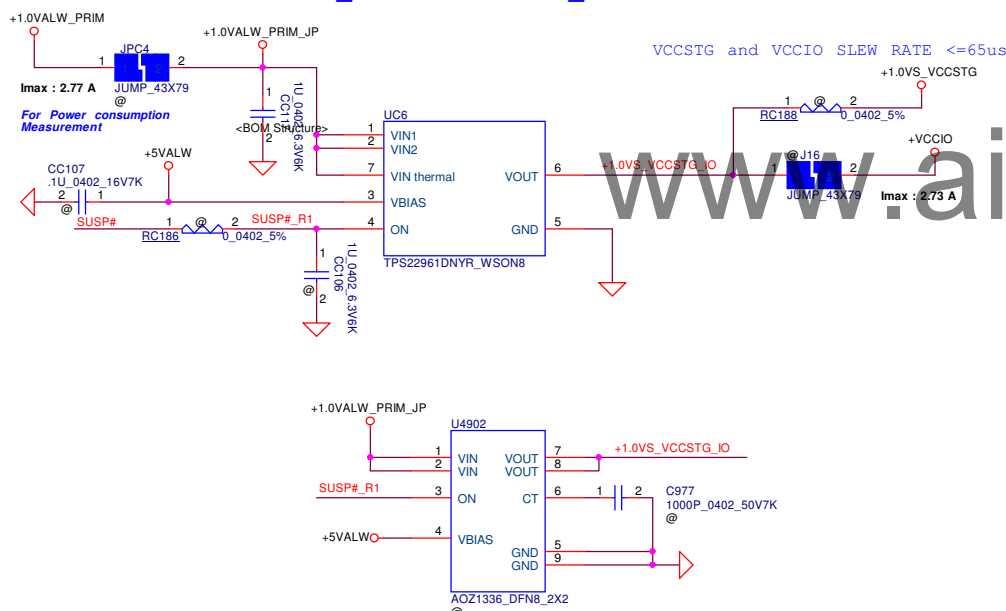
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+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST



+1.8VALW_PRIM TO +1.8VS

+1.0VALW_PRIM TO +1.0VS_VCCSTG

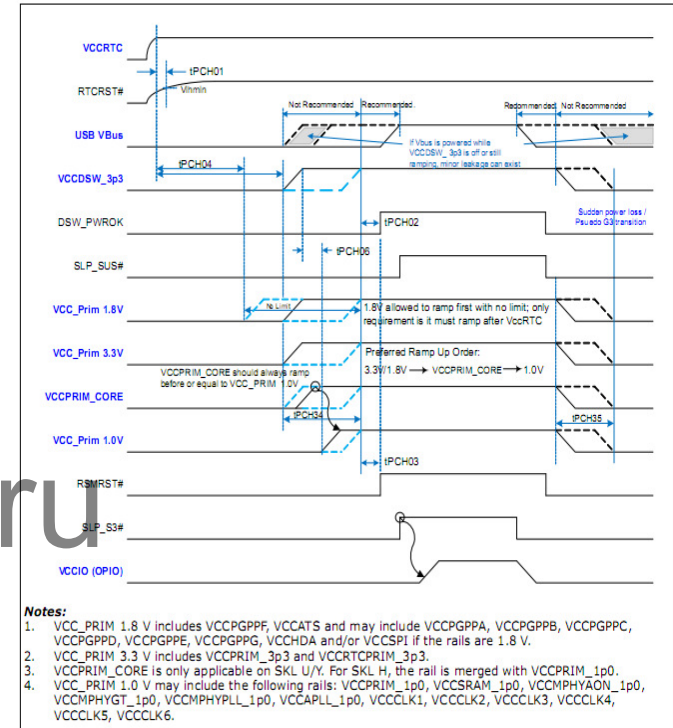


543016_SKL_PDG_1_0
+1.35V_VDDQ_CPU : 2x 10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 10uF 0402 (Placeholder)
3x 22uF 0603

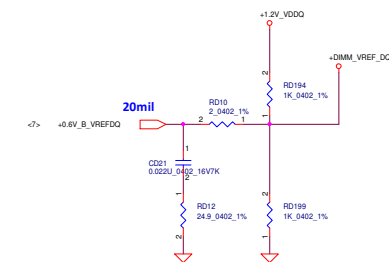
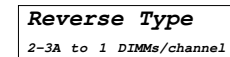
Security Classification			Compal Secret Data			Title		
Issued Date			Deciphered Date			543016_SKL_PDG_1_0		
2017/02/22			2018/02/22			SKL-U(8/12)Power		
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Sheet			13			of		
4			9			54		

UC1P SKL-U Rev. 0.53			UC1Q SKL-U Rev. 0.53			UC1R SKL-U Rev. 0.53		
GND 1 OF 3			GND 2 OF 3			GND 3 OF 3		
A5	VSS	AL65	AT63	VSS	BA49	F8	VSS	L18
A67	VSS	AL66	AT68	VSS	BA53	G10	VSS	L2
A70	VSS	AM13	AT71	VSS	BA57	G22	VSS	L20
AA2	VSS	AM21	AU10	VSS	BA6	G43	VSS	L4
AA4	VSS	AM25	AU15	VSS	BA62	G45	VSS	L8
AA65	VSS	AM27	AU20	VSS	BA66	G48	VSS	N10
AA68	VSS	AM43	AU32	VSS	BA71	G5	VSS	N13
AB15	VSS	AM45	AU38	VSS	BB18	G52	VSS	N19
AB16	VSS	AM46	AV1	VSS	BB26	G55	VSS	N21
AB18	VSS	AM55	AV68	VSS	BB30	G58	VSS	N6
AB21	VSS	AM60	AV69	VSS	BB34	G6	VSS	N65
AB8	VSS	AM61	AV70	VSS	BB38	G60	VSS	N68
AD13	VSS	AM68	AV71	VSS	BB43	G63	VSS	P17
AD16	VSS	AM71	AW10	VSS	BB55	G66	VSS	P19
AD19	VSS	AM8	AW12	VSS	BB6	H15	VSS	P20
AD20	VSS	AN20	AW14	VSS	BB60	H18	VSS	P21
AD21	VSS	AN23	AW16	VSS	BB64	H71	VSS	R13
AD62	VSS	AN28	AW18	VSS	BB67	J11	VSS	R6
AD8	VSS	AN30	AW21	VSS	BB70	J13	VSS	T15
AE64	VSS	AN32	AW23	VSS	C1	J25	VSS	T17
AE65	VSS	AN33	AW26	VSS	C25	J28	VSS	T18
AE66	VSS	AN35	AW28	VSS	C5	J32	VSS	T2
AE67	VSS	AN37	AW30	VSS	D10	J35	VSS	T21
AE68	VSS	AN38	AW32	VSS	D11	J38	VSS	T4
AE69	VSS	AN40	AW34	VSS	D14	J42	VSS	U10
AF1	VSS	AN42	AW36	VSS	D18	J8	VSS	U63
AF10	VSS	AN58	AW38	VSS	D22	K16	VSS	U64
AF15	VSS	AN63	AW41	VSS	D25	K18	VSS	U66
AF17	VSS	AP10	AW43	VSS	D26	K22	VSS	U67
AF2	VSS	AP18	AW45	VSS	D30	K61	VSS	U69
AF4	VSS	AP20	AW47	VSS	D34	K63	VSS	U70
AF63	VSS	AP23	AW49	VSS	D39	K64	VSS	V16
AG16	VSS	AP28	AW51	VSS	D44	K65	VSS	V17
AG17	VSS	AP32	AW53	VSS	D45	K66	VSS	V18
AG18	VSS	AP35	AW55	VSS	D47	K67	VSS	W13
AG19	VSS	AP38	AW57	VSS	D48	K68	VSS	W6
AG20	VSS	AP42	AW6	VSS	D53	K70	VSS	W6
AG21	VSS	AP58	AW60	VSS	D58	K71	VSS	Y17
AG71	VSS	AP63	AW62	VSS	D6	L11	VSS	Y18
AH13	VSS	AP68	AW64	VSS	D62	L16	VSS	Y20
AH6	VSS	AP70	AW66	VSS	D66	L17	VSS	Y21
AH63	VSS	AR11	AW8	VSS	D69	E11	VSS	
AH64	VSS	AR15	AY66	VSS	E15	E18	VSS	
AH67	VSS	AR16	B10	VSS	E21	E21	VSS	
AJ15	VSS	AR20	B14	VSS	E46	E50	VSS	
AJ18	VSS	AR23	B18	VSS	E53	E53	VSS	
AJ20	VSS	AR28	B22	VSS	E56	E56	VSS	
AJ4	VSS	AR35	B30	VSS	E6	E6	VSS	
AK11	VSS	AR42	B34	VSS	E65	E71	VSS	
AK16	VSS	AR43	B39	VSS	E71	F1	VSS	
AK18	VSS	AR45	B44	VSS	F13	F23	VSS	
AK21	VSS	AR46	B48	VSS	F22	F22	VSS	
AK22	VSS	AR48	B53	VSS	F23	F23	VSS	
AK27	VSS	AR5	B58	VSS	F27	F27	VSS	
AK63	VSS	AR50	B62	VSS	F28	F28	VSS	
AK68	VSS	AR52	B66	VSS	F32	F32	VSS	
AK69	VSS	AR53	B71	VSS	F33	F33	VSS	
AK8	VSS	AR55	BA1	VSS	F35	F35	VSS	
AL2	VSS	AR58	BA10	VSS	F37	F37	VSS	
AL28	VSS	AR63	BA14	VSS	F38	F38	VSS	
AL32	VSS	AR6	BA18	VSS	F4	F4	VSS	
AL35	VSS	AT2	BA2	VSS	F40	F40	VSS	
AL38	VSS	AT20	BA23	VSS	F42	F42	VSS	
AL4	VSS	AT23	BA28	VSS	BA41		VSS	
AL45	VSS	AT28	BA32	VSS			VSS	
AL48	VSS	AT35	BA36	VSS			VSS	
AL52	VSS	AT4	F68	VSS			VSS	
AL55	VSS	AT42	AT56	VSS			VSS	
AL58	VSS	AT58		VSS			VSS	
AL64	VSS			VSS			VSS	

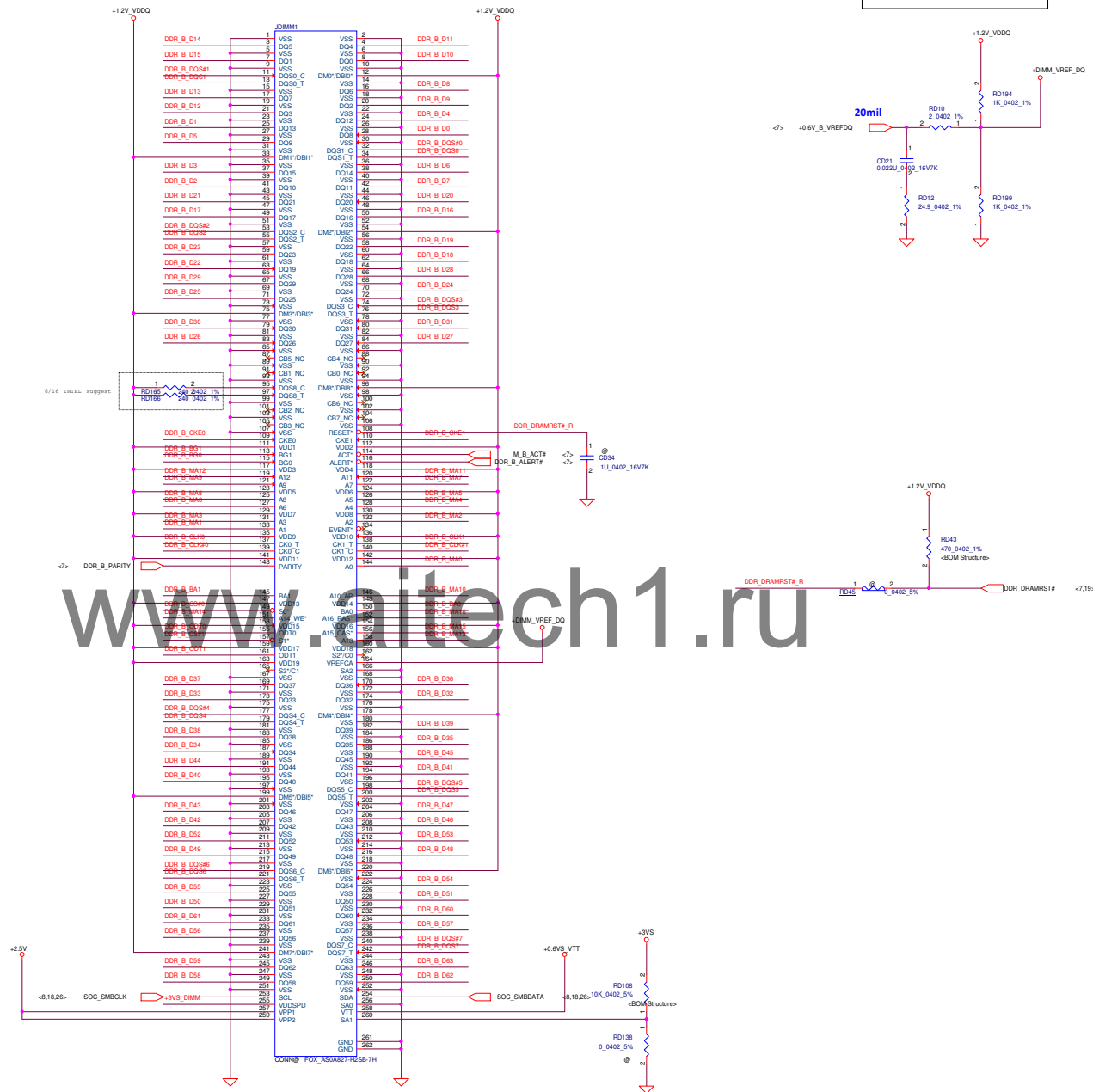
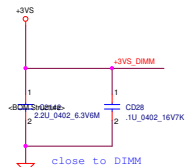
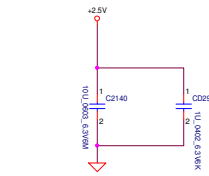
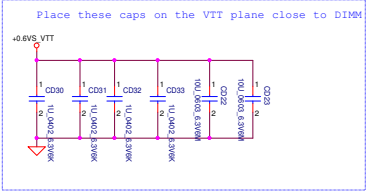
Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System



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				Date: Friday, June 09, 2017		
				Sheet	16	of 54



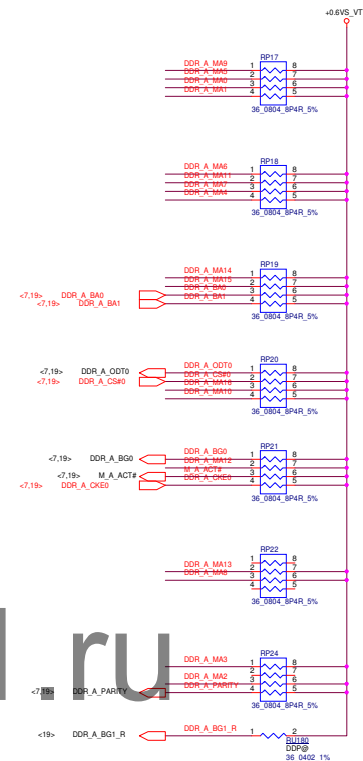
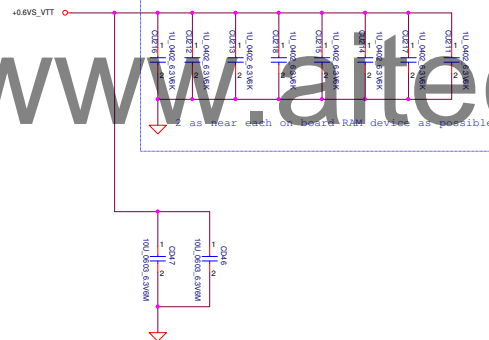
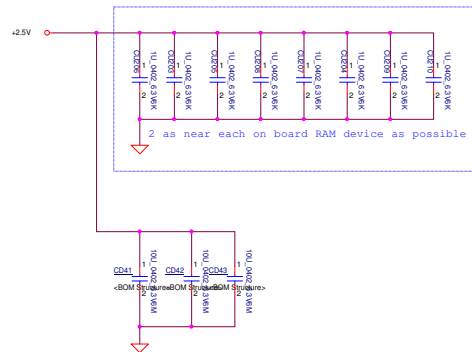
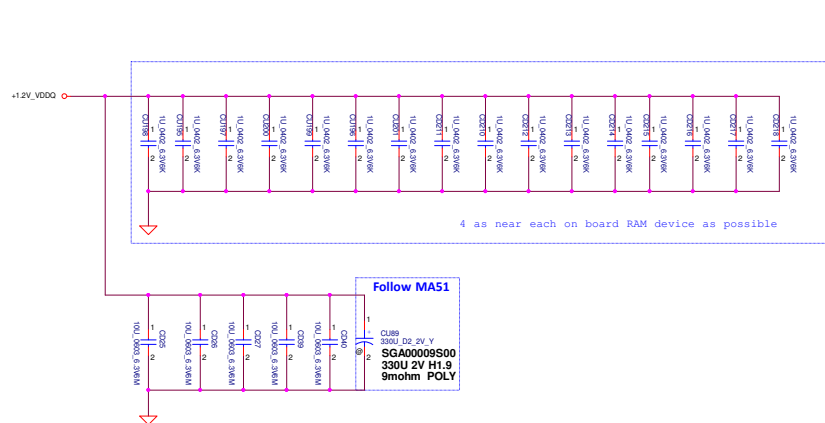
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket



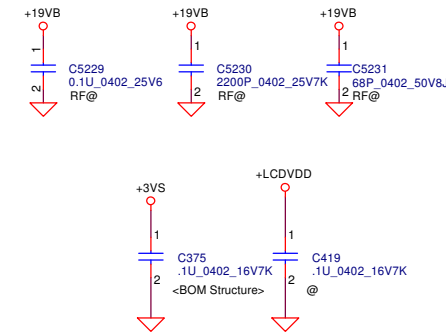
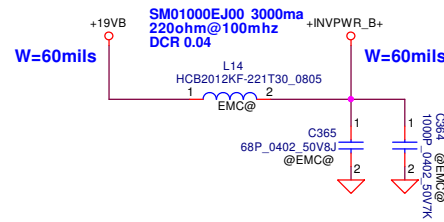
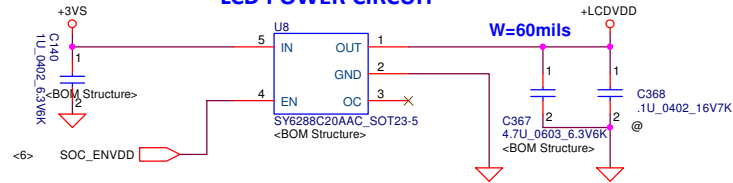
Interleaved Memory

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				Sheet	18 of 54

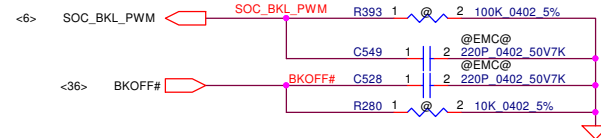
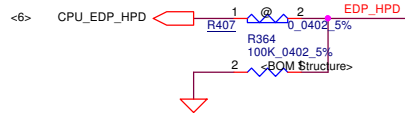
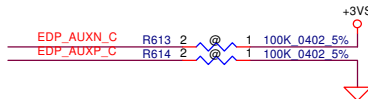
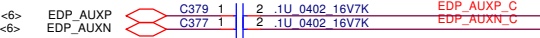
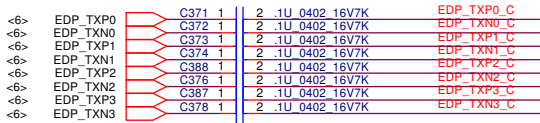
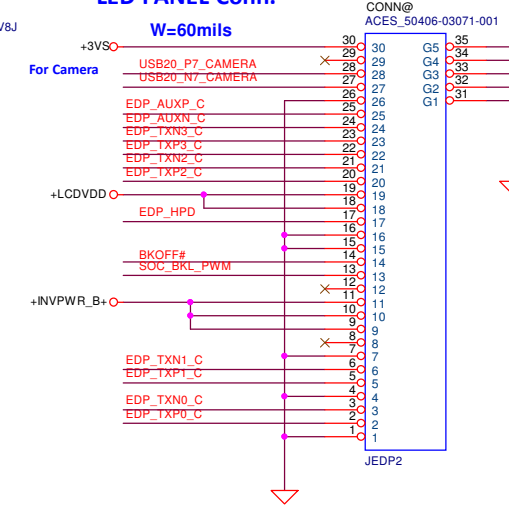
<7.19> DOR_A_MA0..16



LCD POWER CIRCUIT



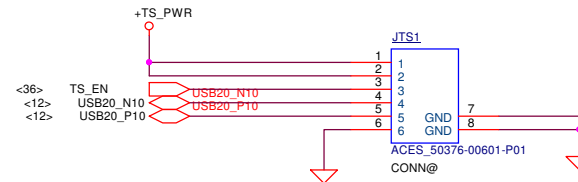
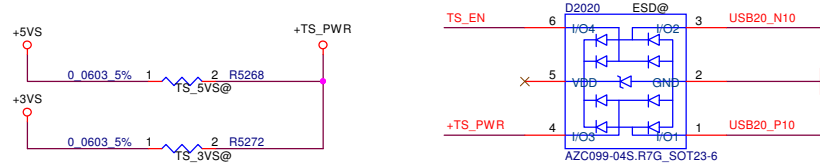
LED PANEL Conn.



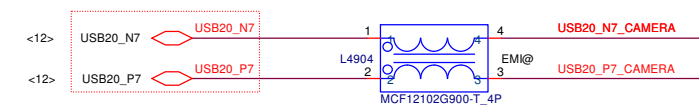
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SP010011Z00

Touch Screen Conn.



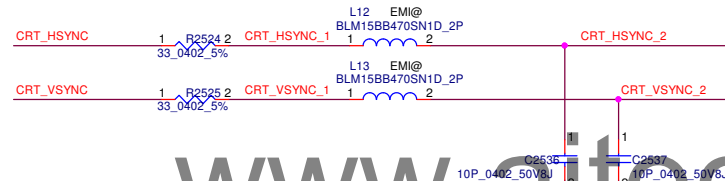
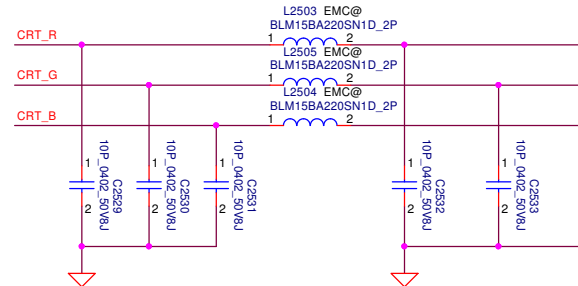
Camera



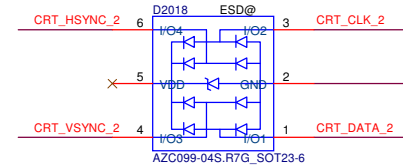
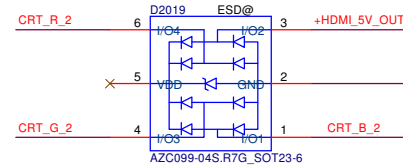
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						LA-F241P					

CRT conn.

SM01000LU00 (S SUPPRE_MURATA BLM15BA220SN1D 0402)



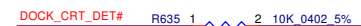
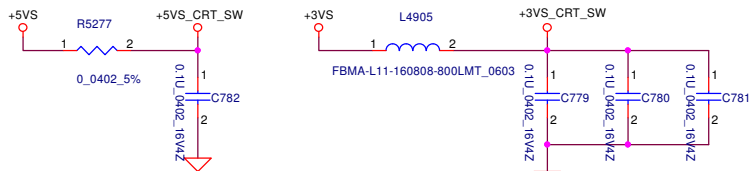
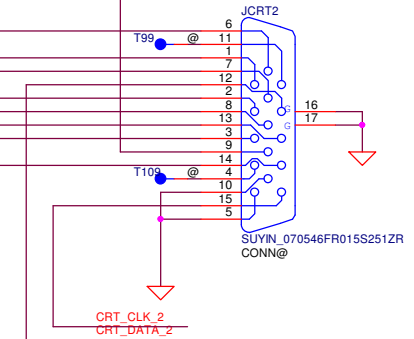
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W=40mils

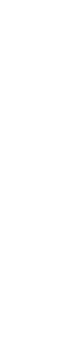
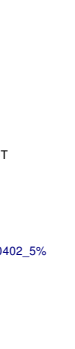
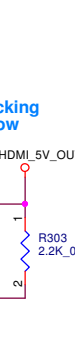
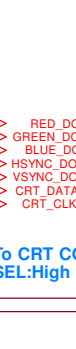
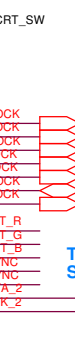
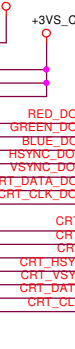
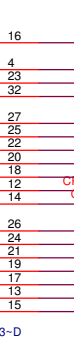
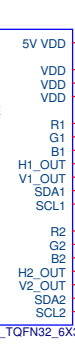
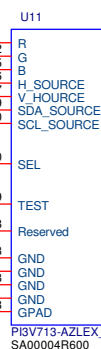
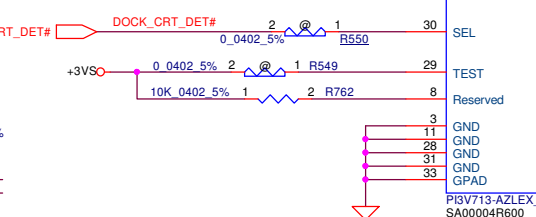
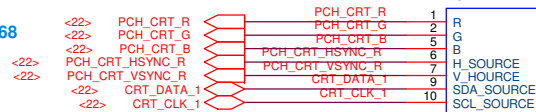
+HDMI_5V_OUT

CRT Connector

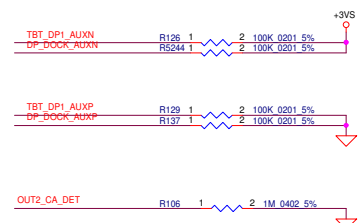
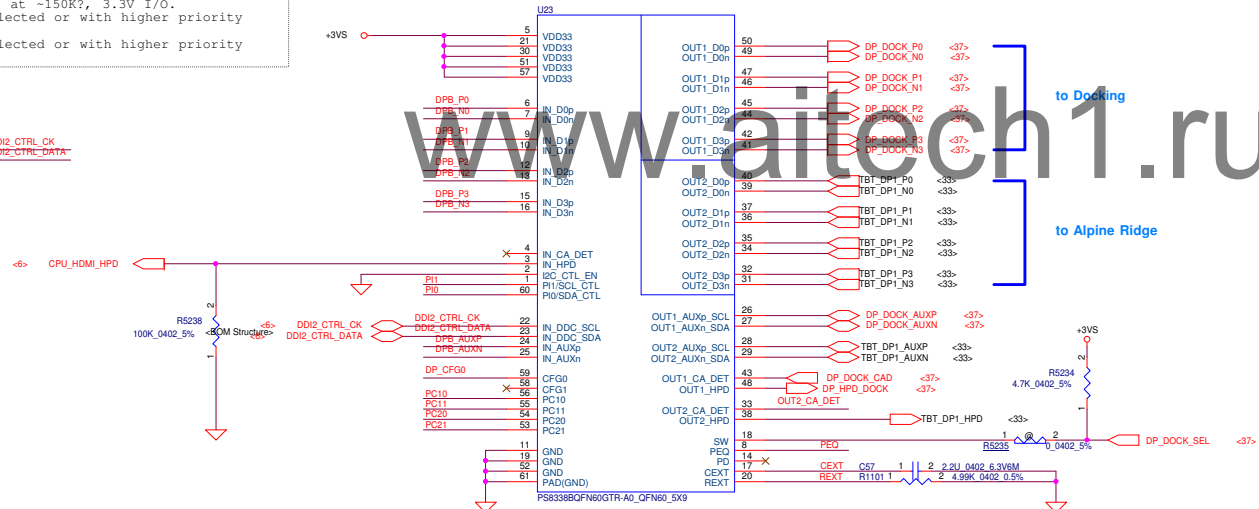
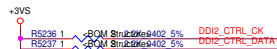
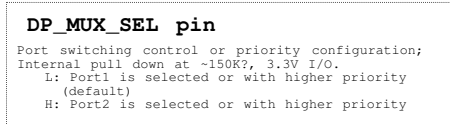
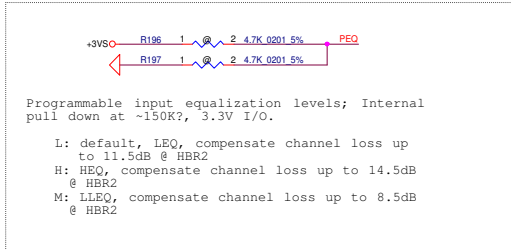
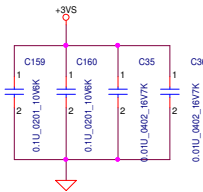
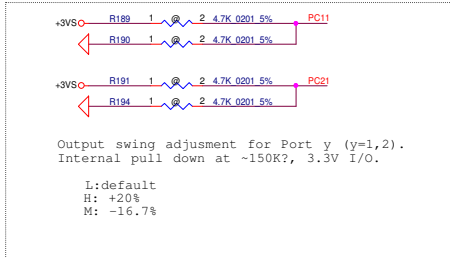
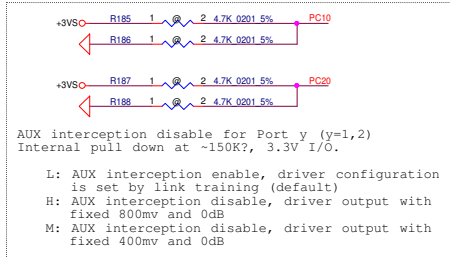
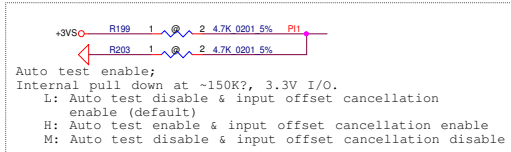
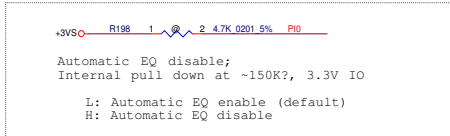
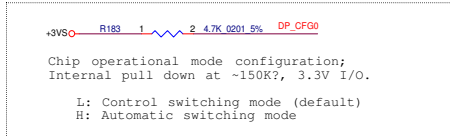


SELx	Function
L	port 1 is chose
H	port 2 is chose

From RTD2168

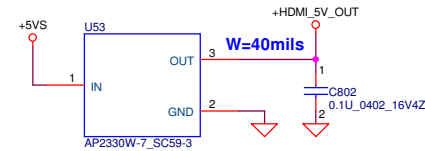
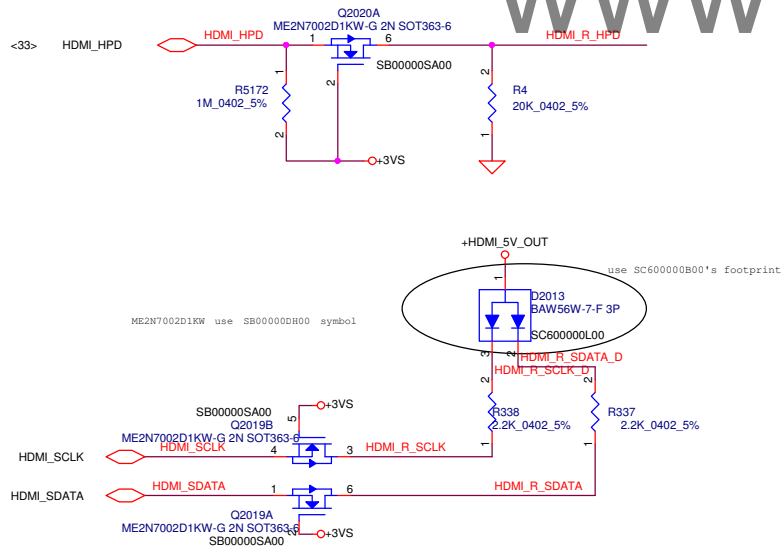
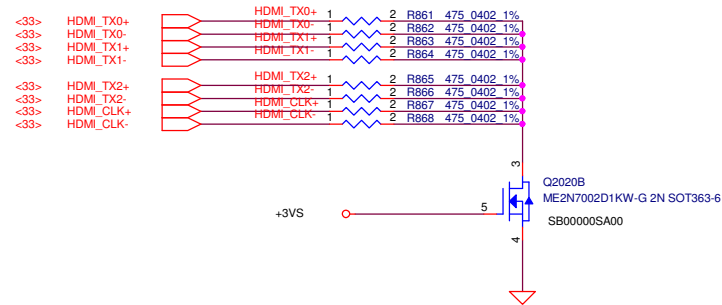


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Size	Document Number	Rev		0.1	
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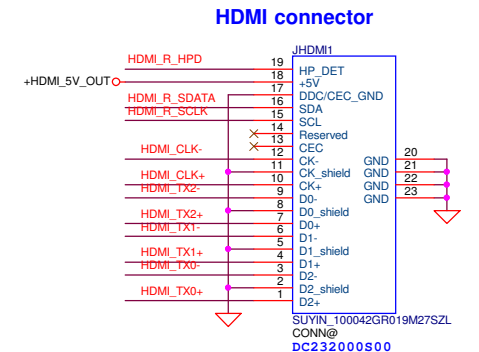
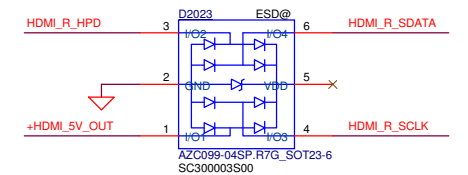
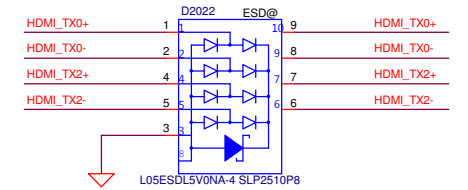
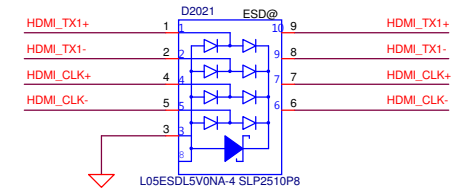


CPU_DP2_N0	CPU_DP2_N0	C300	2	1	0.1U 0402 16V7K	DPB_N0
CPU_DP2_P0	CPU_DP2_P0	C299	2	1	0.1U 0402 16V7K	DPB_P0
CPU_DP2_N1	CPU_DP2_N1	C277	2	1	0.1U 0402 16V7K	DPB_N1
CPU_DP2_P1	GPU_DP2_P1	C278	2	1	0.1U 0402 16V7K	DPB_P1
CPU_DP2_N2	GPU_DP2_N2	C276	2	1	0.1U 0402 16V7K	DPB_N2
CPU_DP2_P2	GPU_DP2_P2	C301	2	1	0.1U 0402 16V7K	DPB_P2
CPU_DP2_N3	GPU_DP2_N3	C298	2	1	0.1U 0402 16V7K	DPB_N3
CPU_DP2_P3	GPU_DP2_P3	C302	2	1	0.1U 0402 16V7K	DPB_P3
DD12_AUX_DN	DD12_AUX_DN	C285	2	1	0.1U 0402 16V7K	DPB_AUXN
DD12_AUX_DP	DD12_AUX_DP	C289	2	1	0.1U 0402 16V7K	DPB_AUXP

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				Size Document Number
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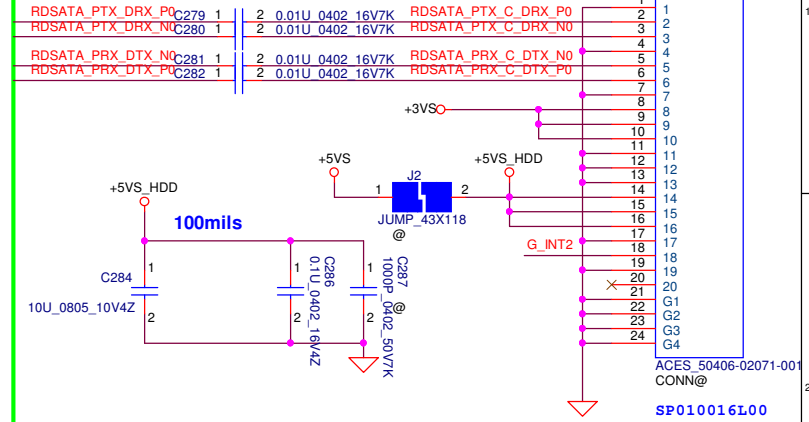
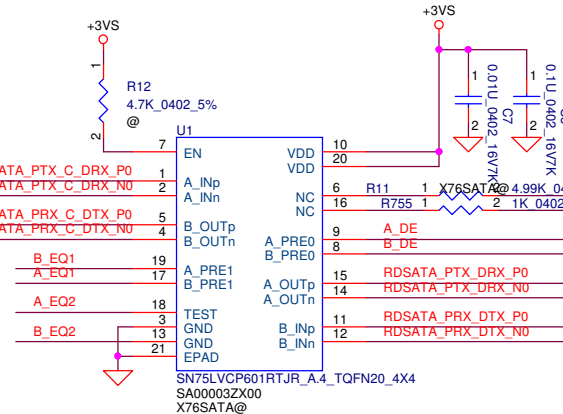
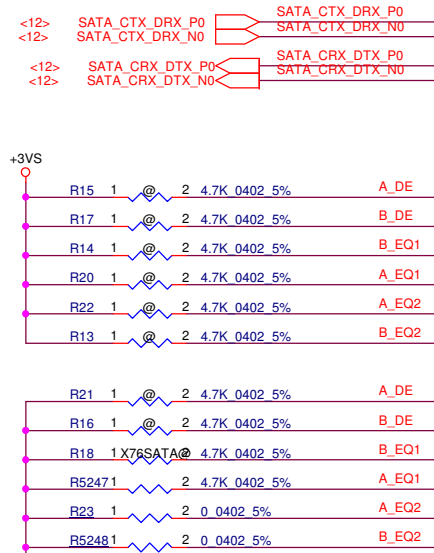
2017/4/17 add diode for ESD request



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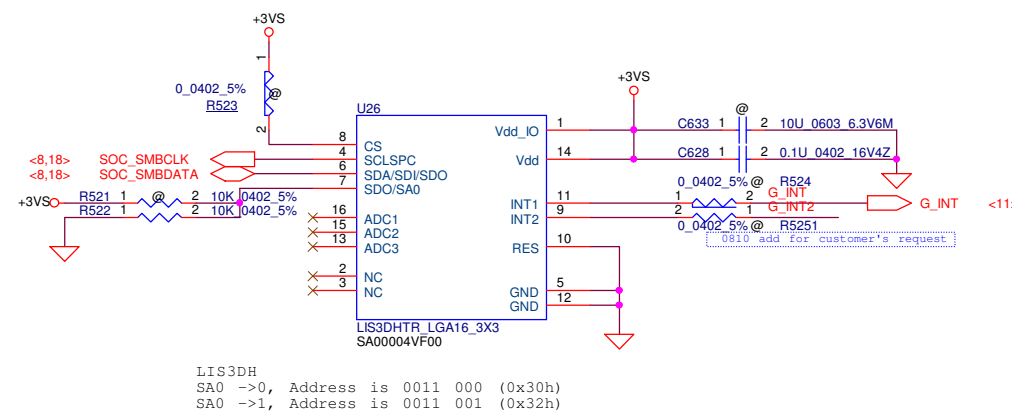
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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HDD Board Conn

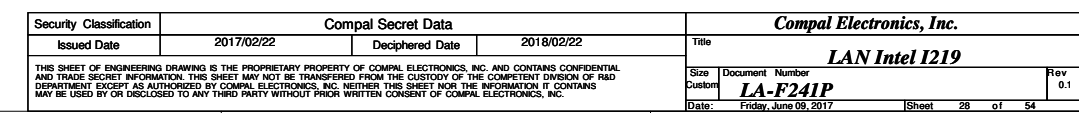


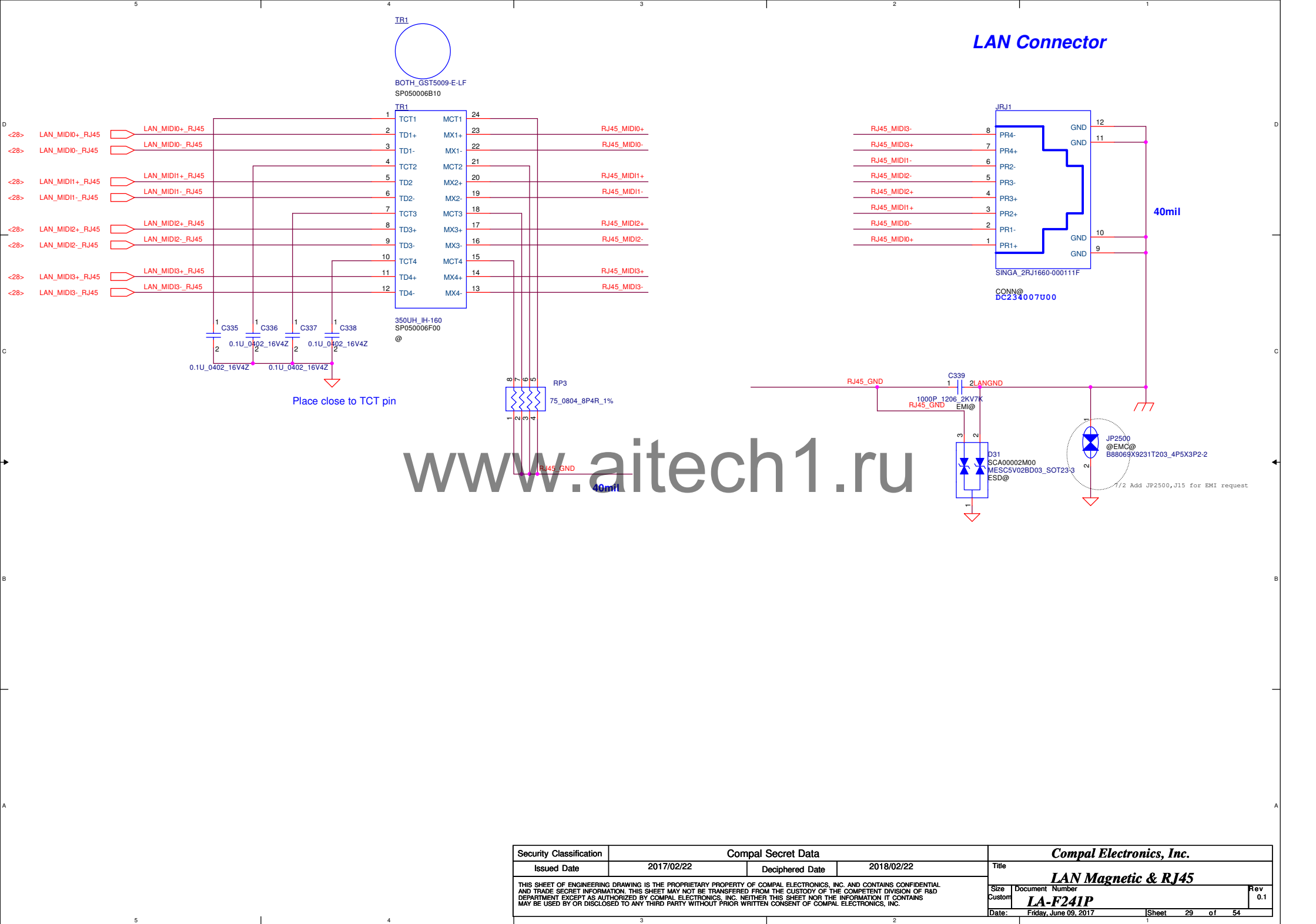
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APS G-Sensor

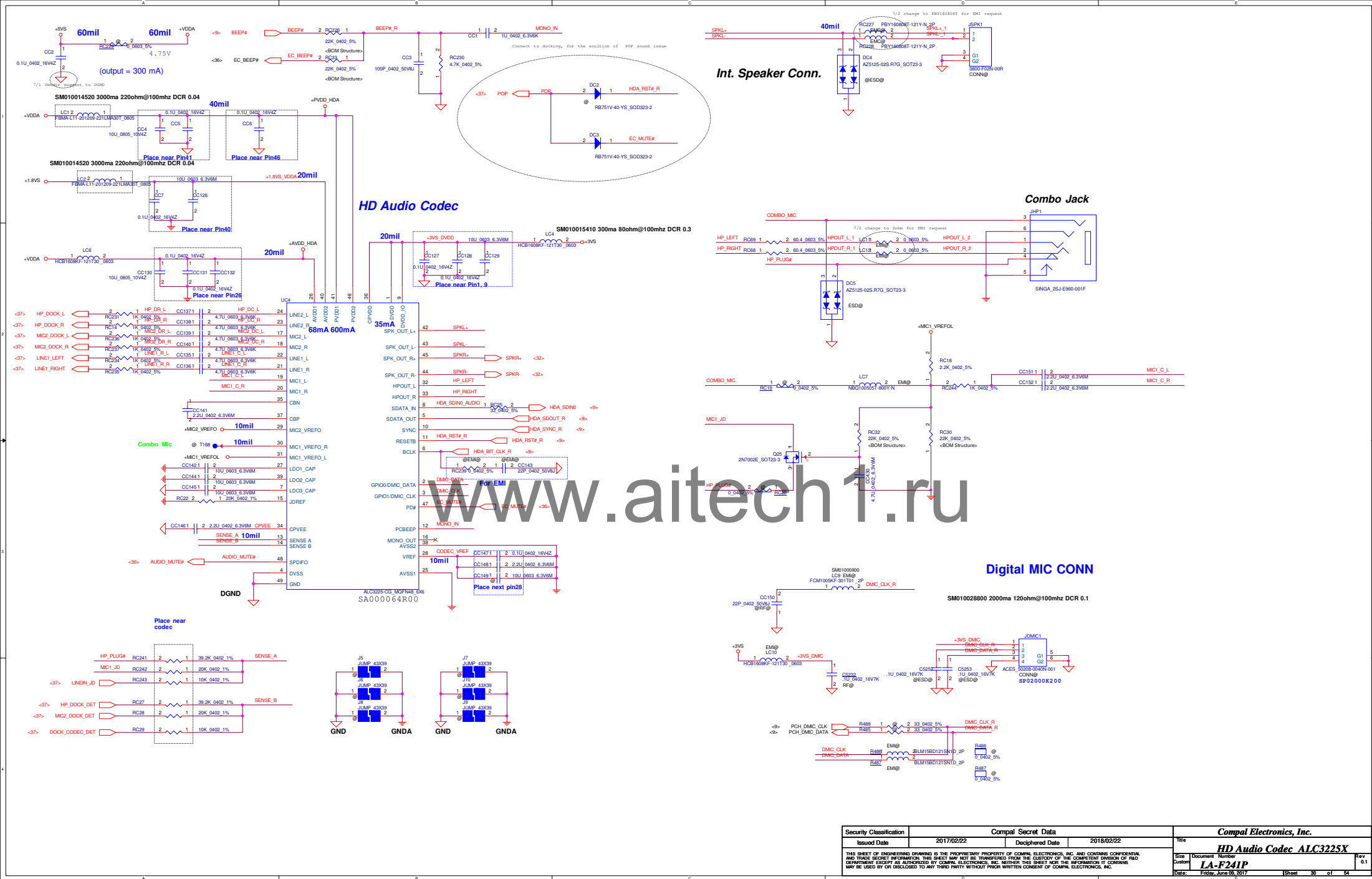


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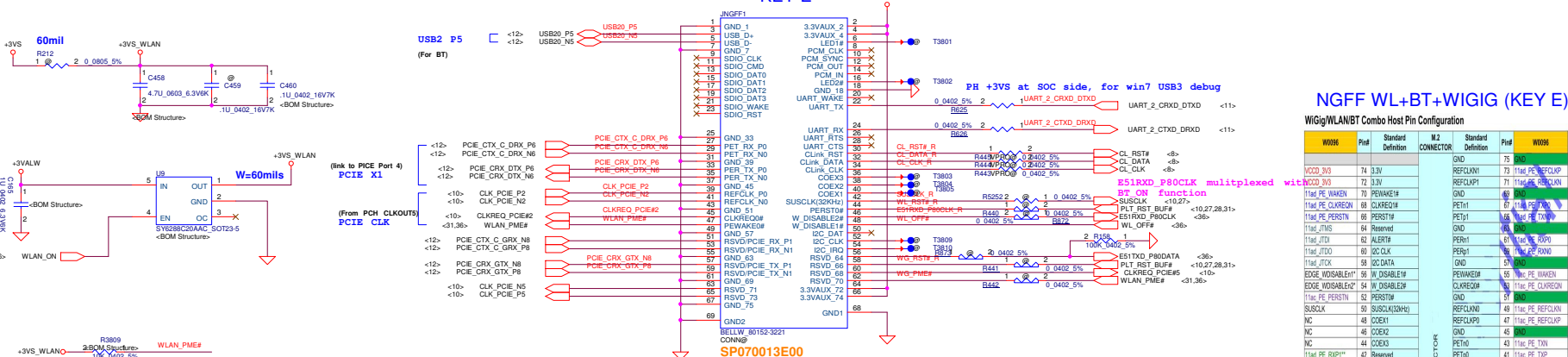


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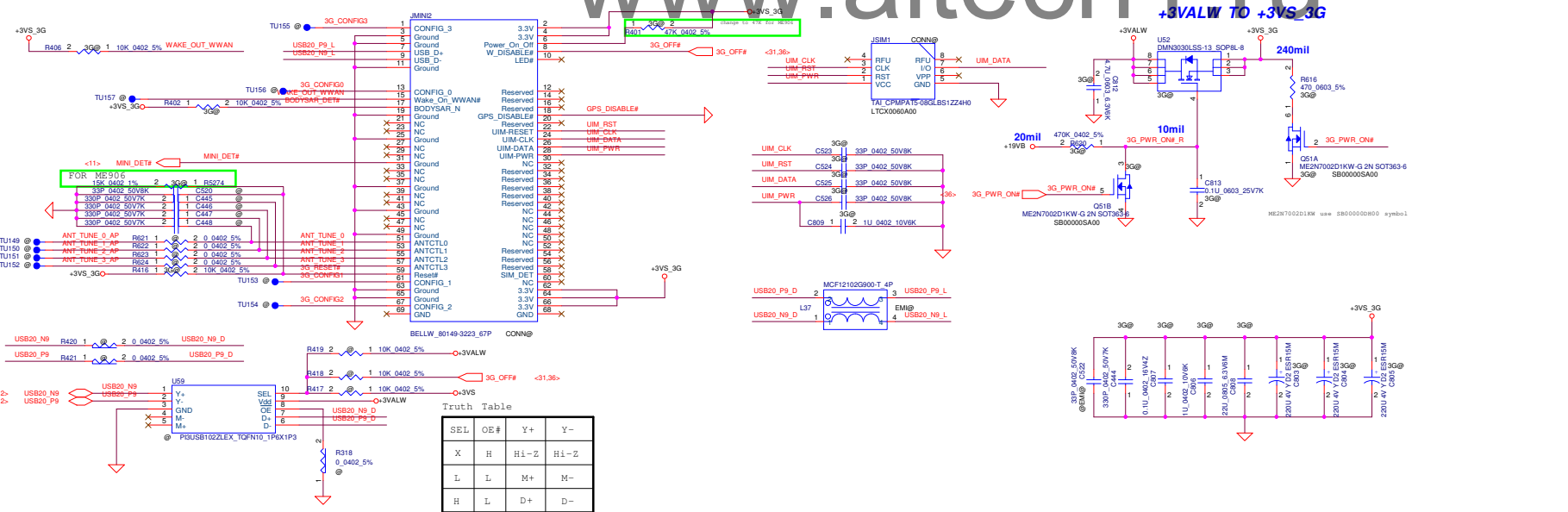
Wireless LAN



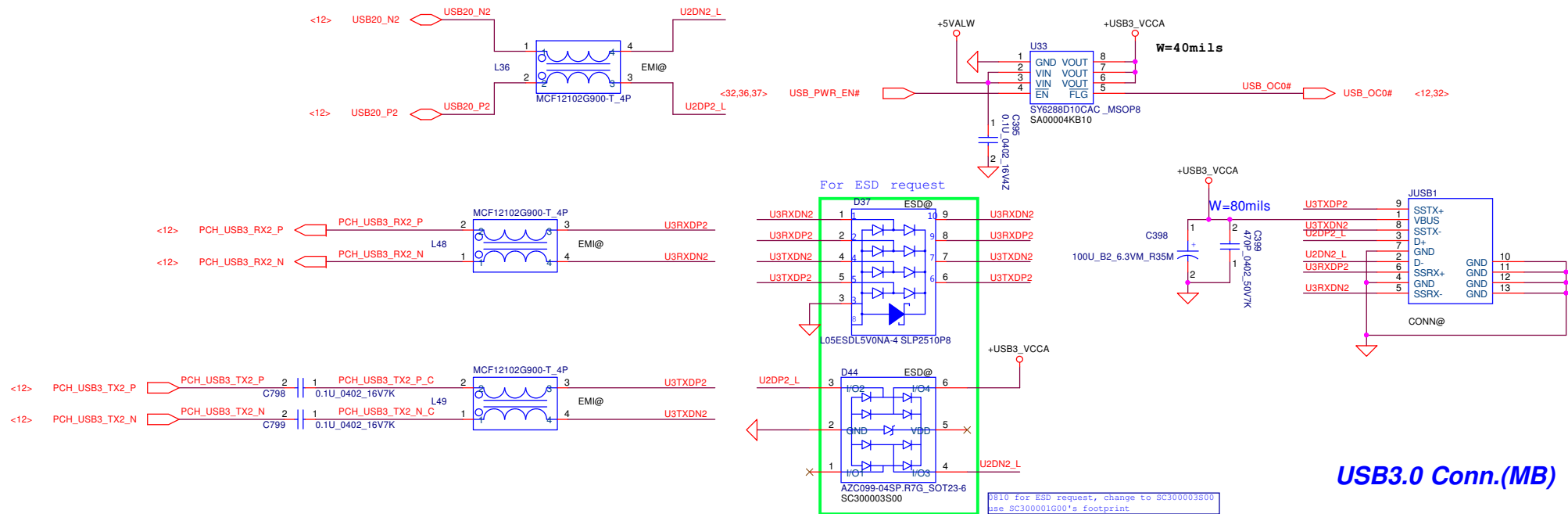
3.1.8.1.3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

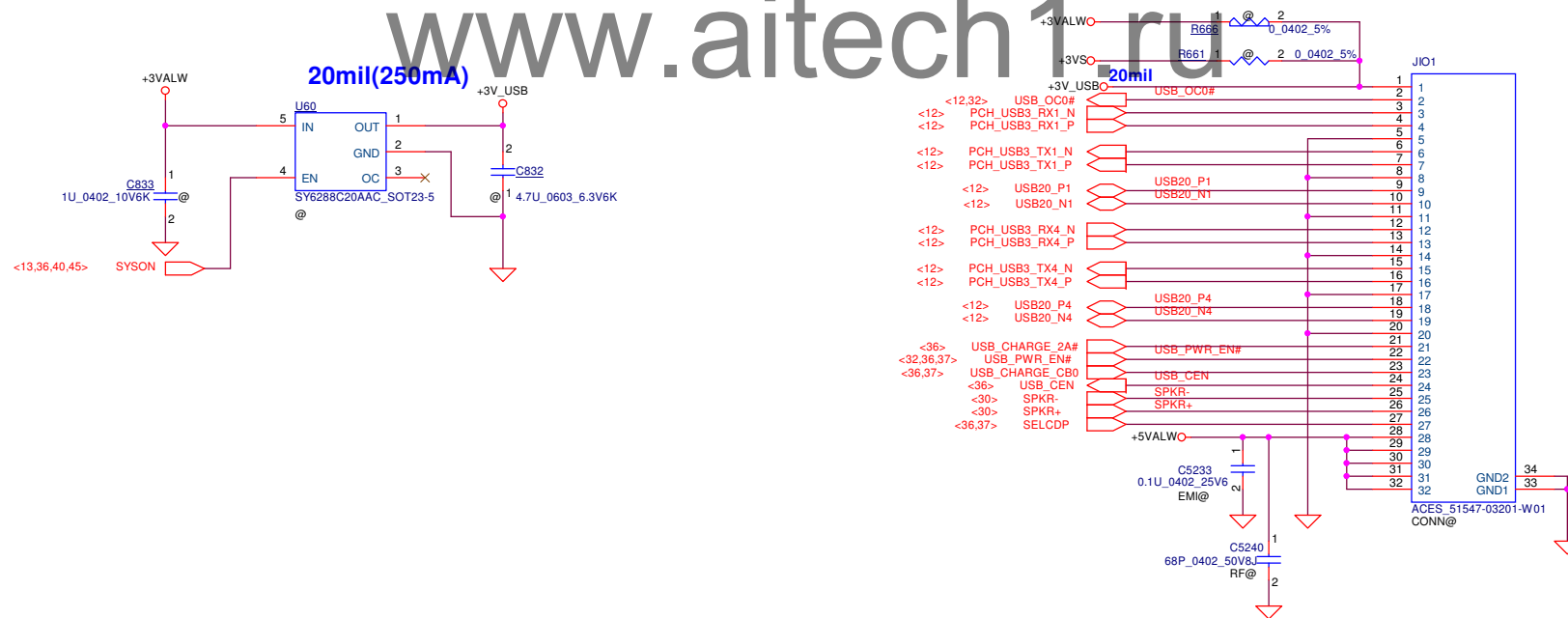
- ❑ **RD_X** **UART_RSD** (Input): Receive Data
- ❑ **RT_X** **UART_TXD** (Output): Transmit Data
- ❑ **RTS** **UART_RTS** (Input): Request to Send (Host Flow Control)
- ❑ **CTS** **UART_CTS** (Output): Clear to Send (Device Flow Control)
- ❑ **Host Wake-Up** **UART_Wake#** (Output): Host wake-up line is optional in case the host support in-band wake-up



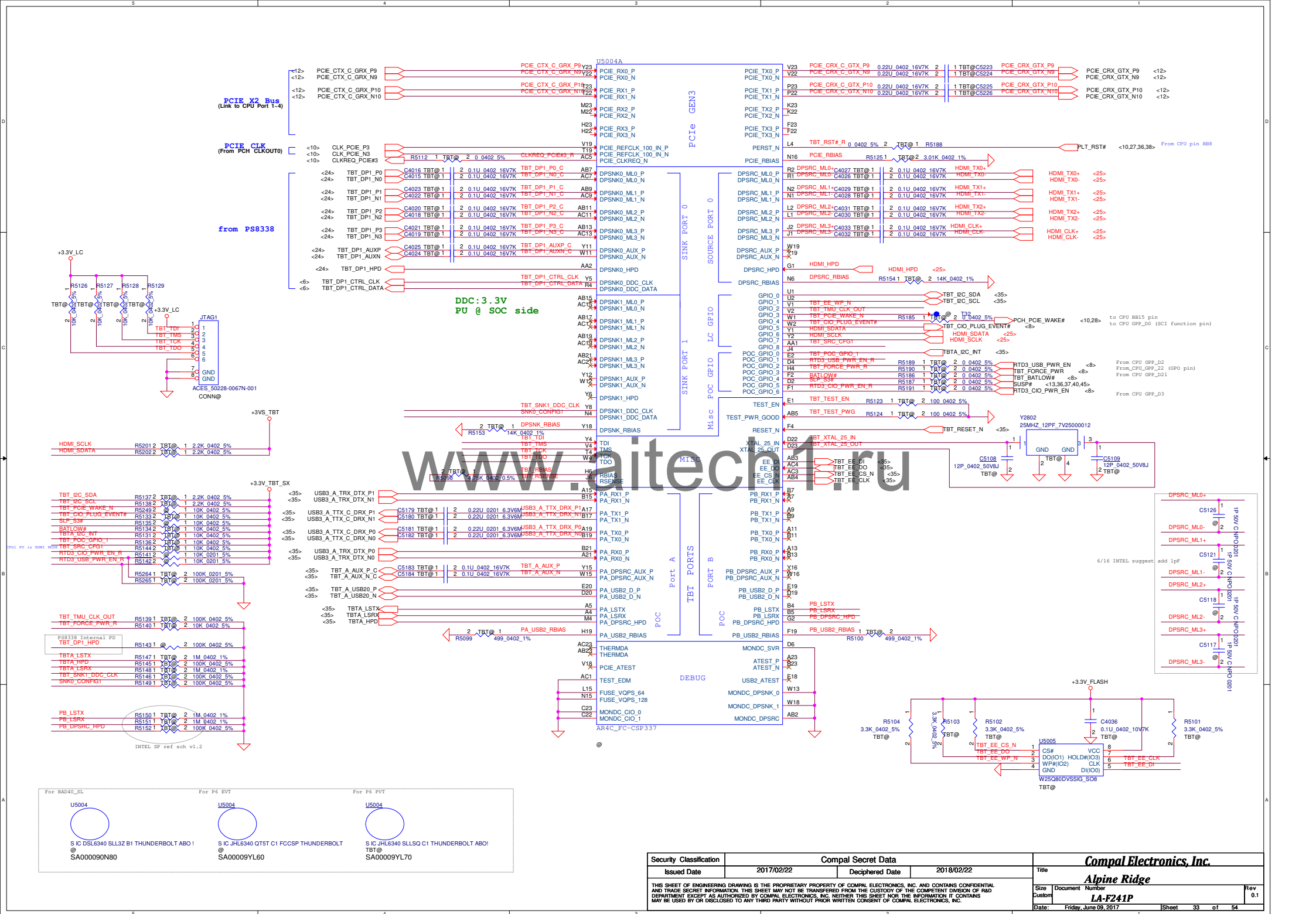
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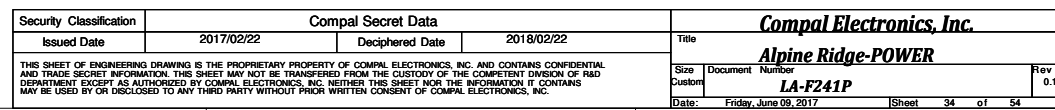
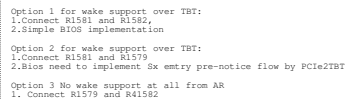


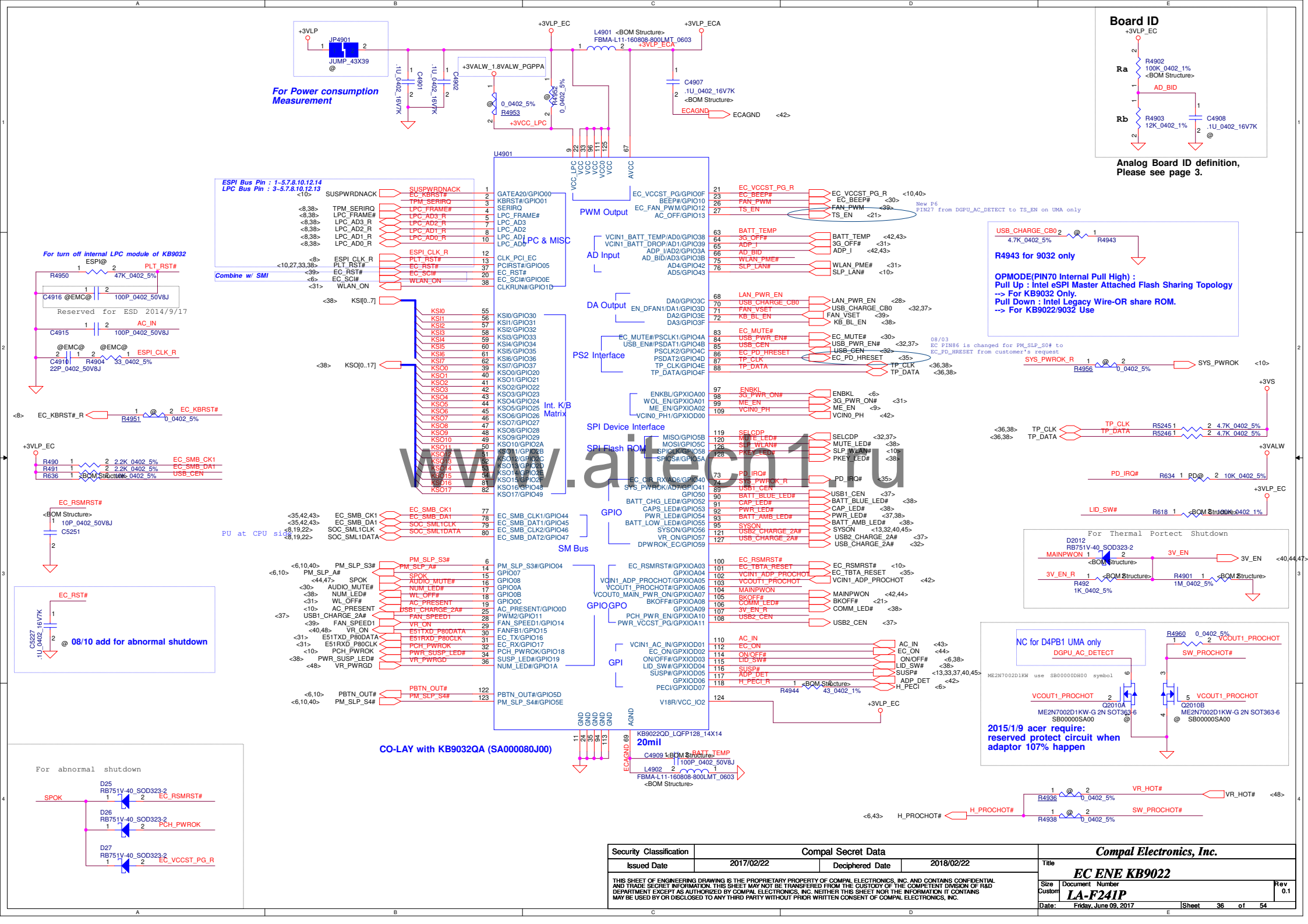
IO Board Conn(For FFC,FPC)



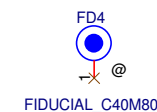
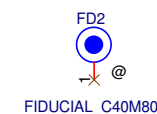
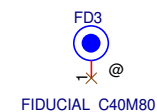
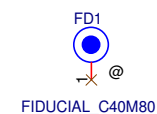
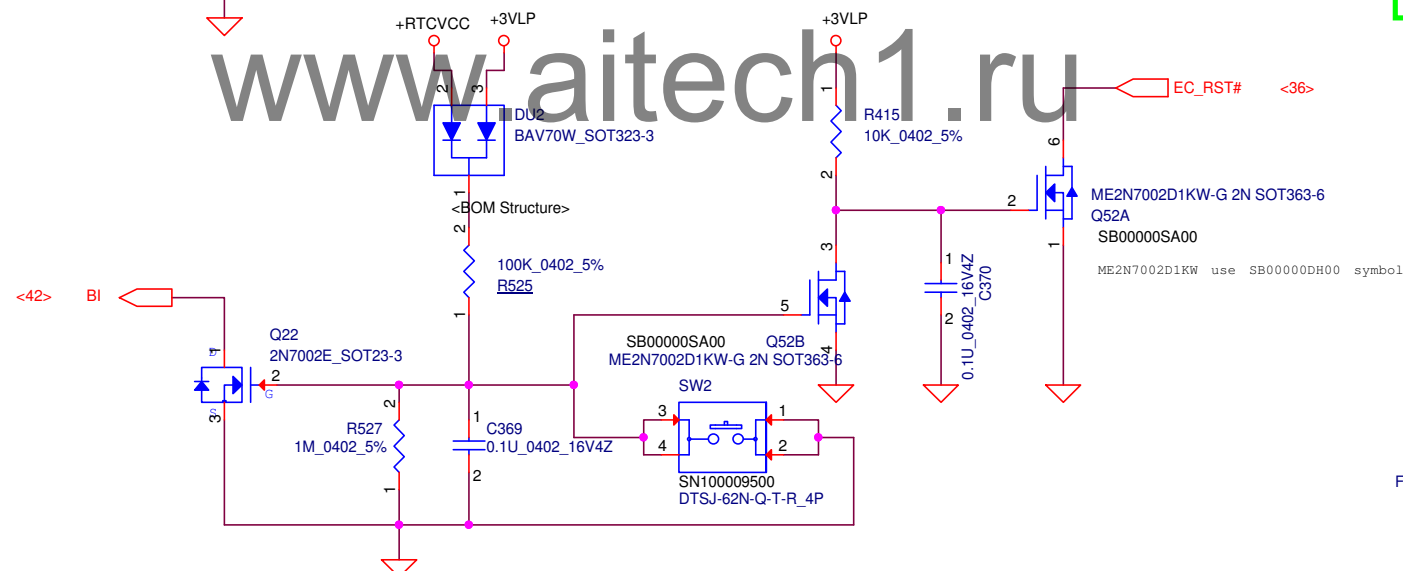
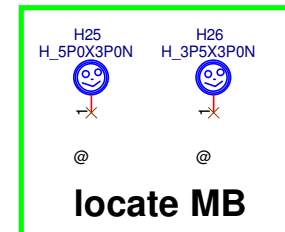
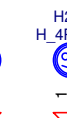
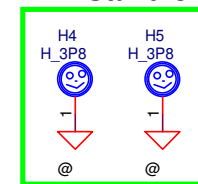
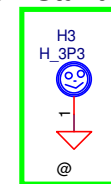
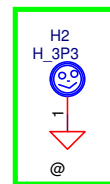
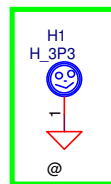
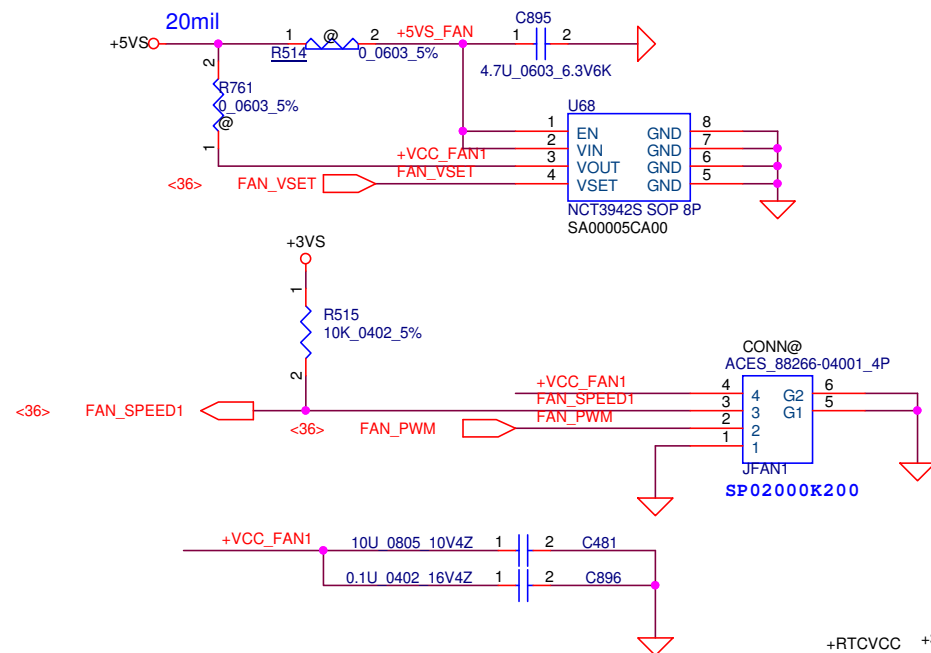
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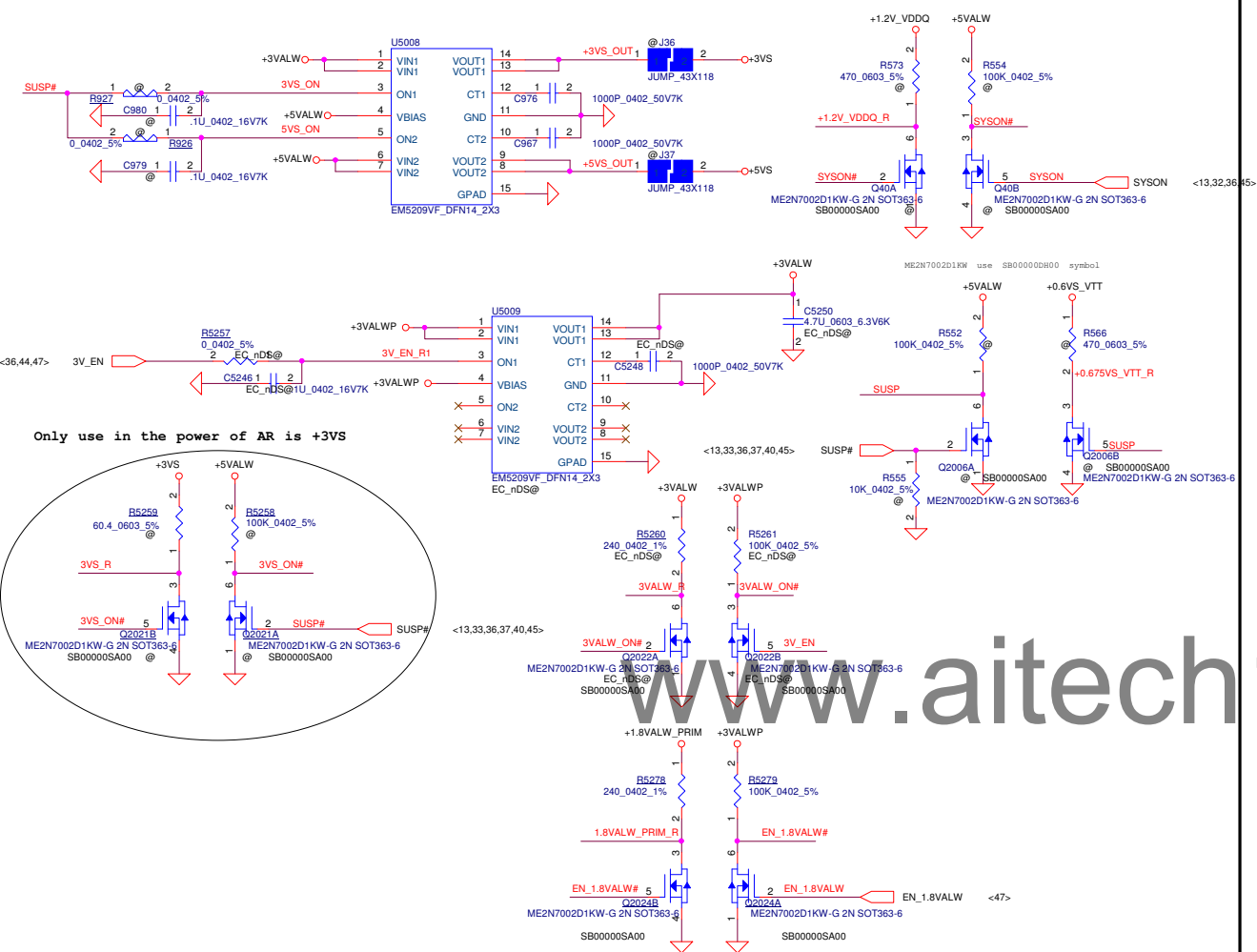


FAN Conn

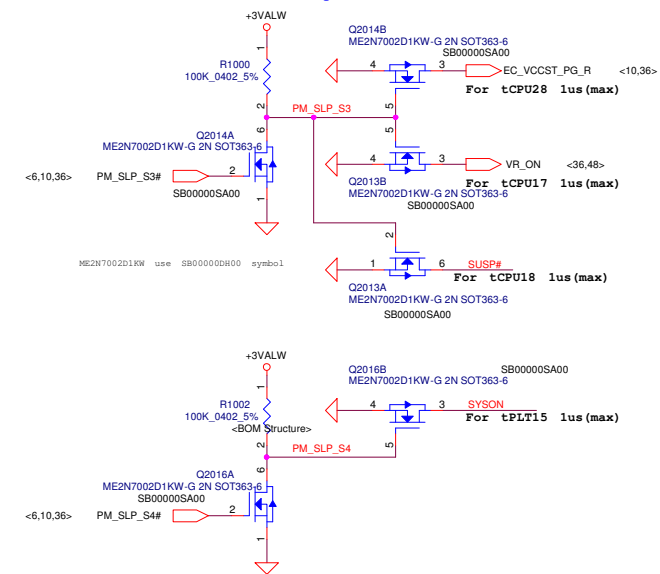


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				Size	Document Number	Rev
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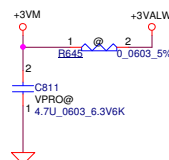
DC & VGA Interface



For Power Of f Sequence

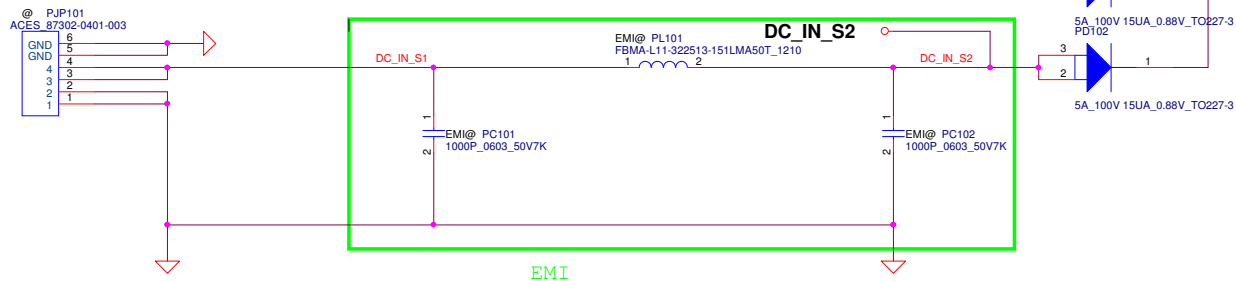


+3VALW to +3VM for Intel AMT
20mil(68mA)



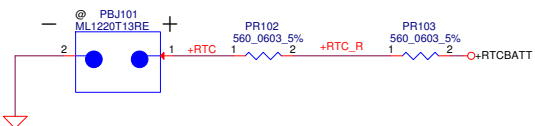
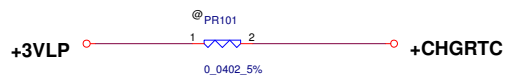
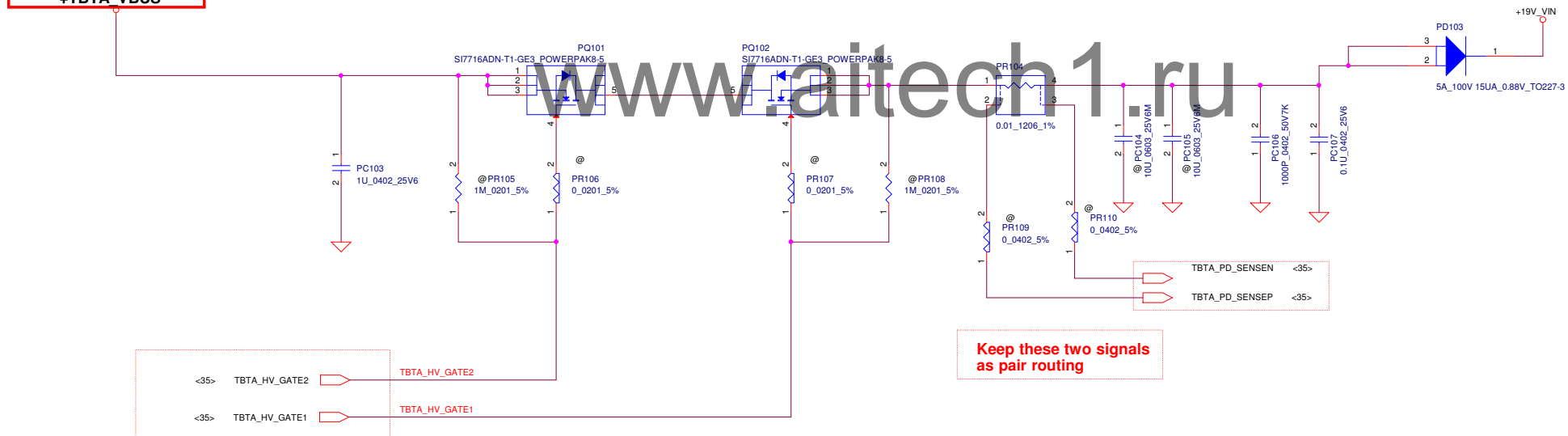
联想 华硕笔记本主板交换 type-c转接头
出售 维销管家信息管理系统出售 需要
联系微信 yangyang51241

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				Size	Document Number
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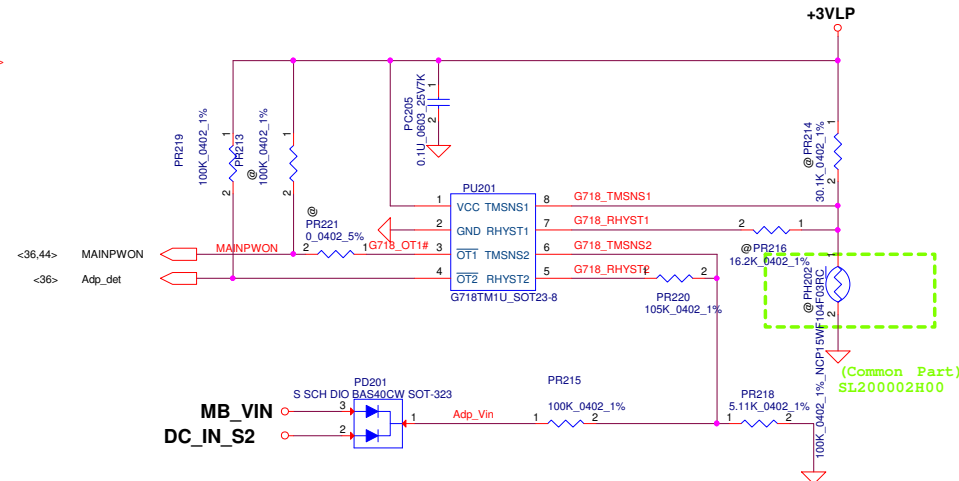
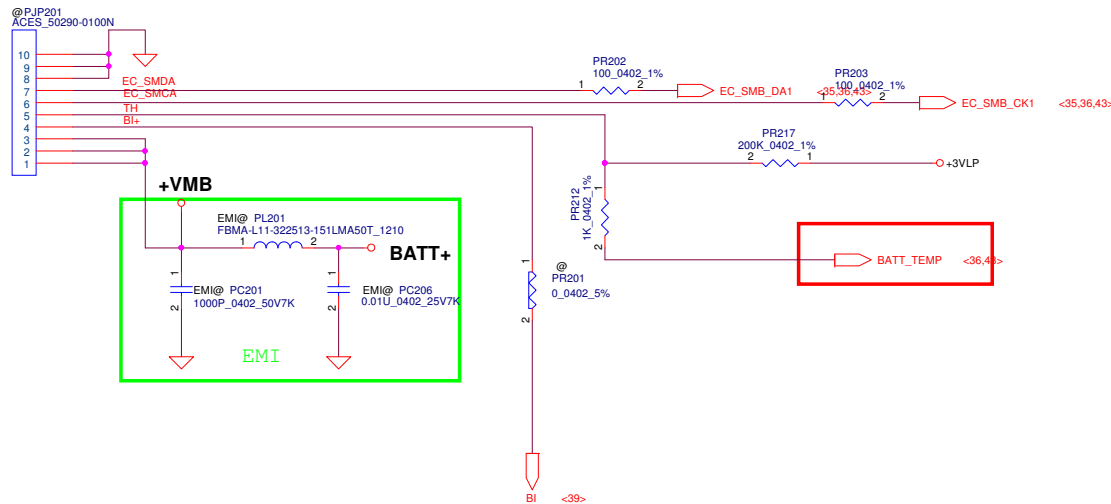
2015/7/8
PD101 and PD102 SCS00002F00 change to SCS00002M00

+TBTA_VBUS



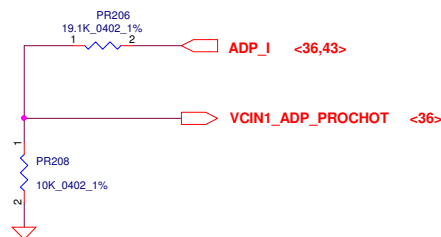
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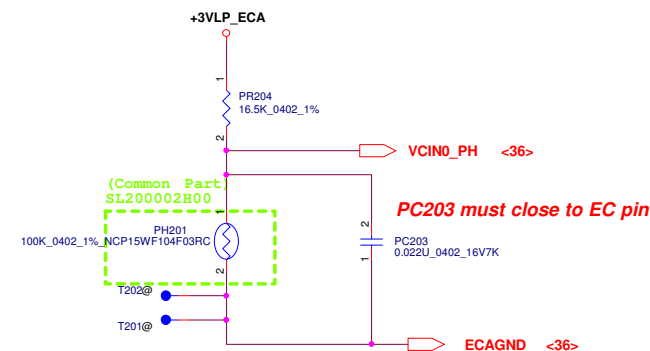


2015/07/09 update

For KB9022 sense 20mΩ	Active	Recovery
65W For AC IN	84.5W, 0.61V	84.5W, 0.61V
45W For PD IN	58.5W, 0.40V	58.5W, 0.40V

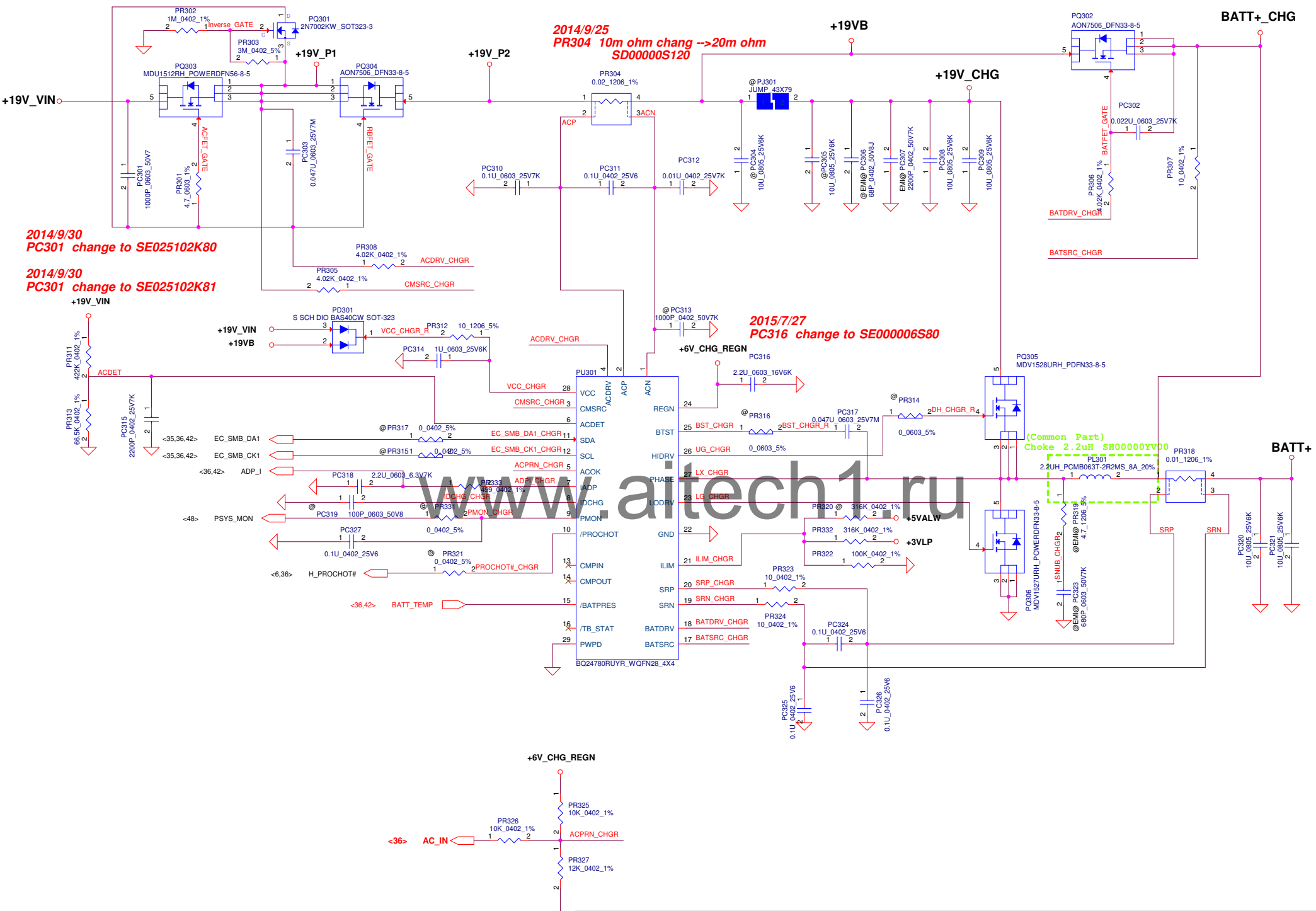


T202 T201 must close to PH201



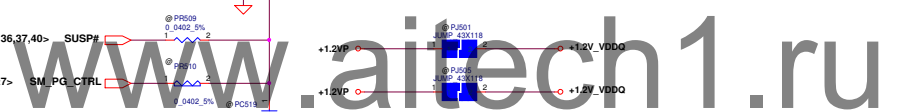
PH1 under CPU bottom side :
CPU thermal protection at 93 +/-3 degree C
Recovery at 56 +/-3 degree C

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						Size	Document Number		Rev
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RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer



```
Mode  Level  +0.675VSP  VTTREF_1.35V
S5    L      off      off
S3    L      off      on
S0    H      on       on

Note: S3 - sleep ; S5 - power off
```

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

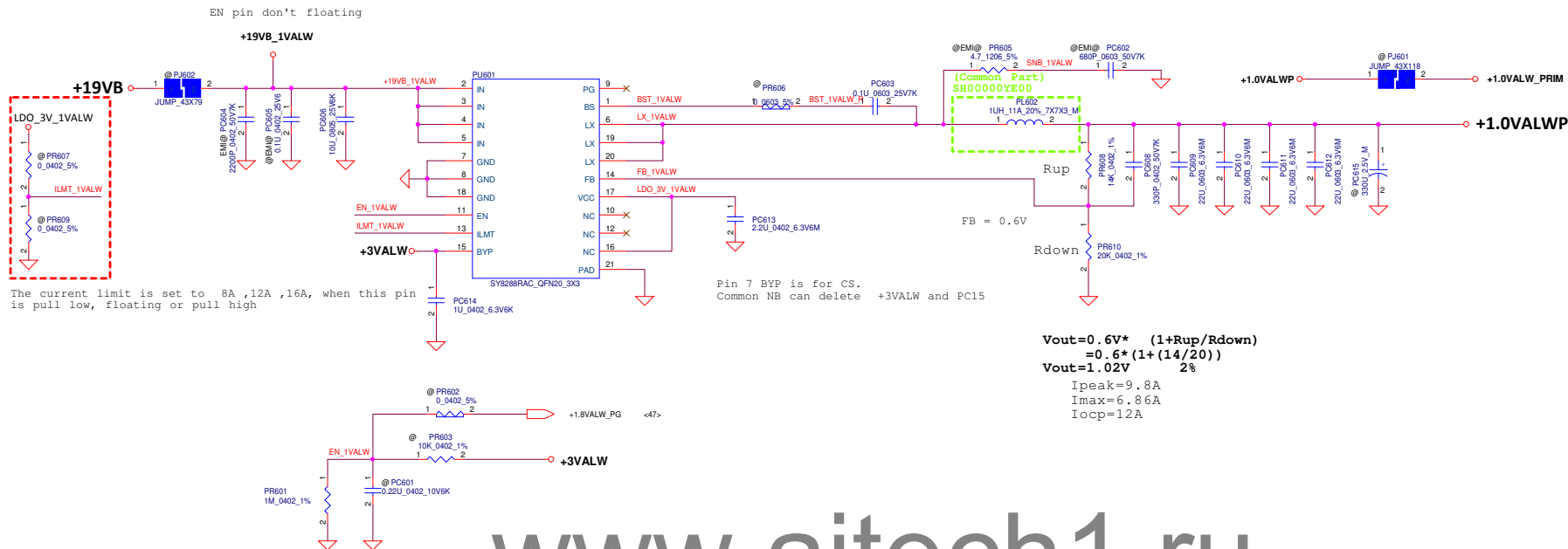
L/S Rds(on): 13.5mohm(Typ), 16.5mohm(Max)
Idsm: 12A@Ta=25C, 9.5A@Ta=70C

Choke: 7x7x3
Rdc=14mohm (Typ), 15mohm (Max)

Switching Frequency: 285kHz
Ipeak=8A
Iocp~9.6A
OVP: 110%~120%
VFB=0.75V, Vout=1.2V
MOSFET footprint: SIS412DN

5/29 add PC526
In order to avoid capacitor decay

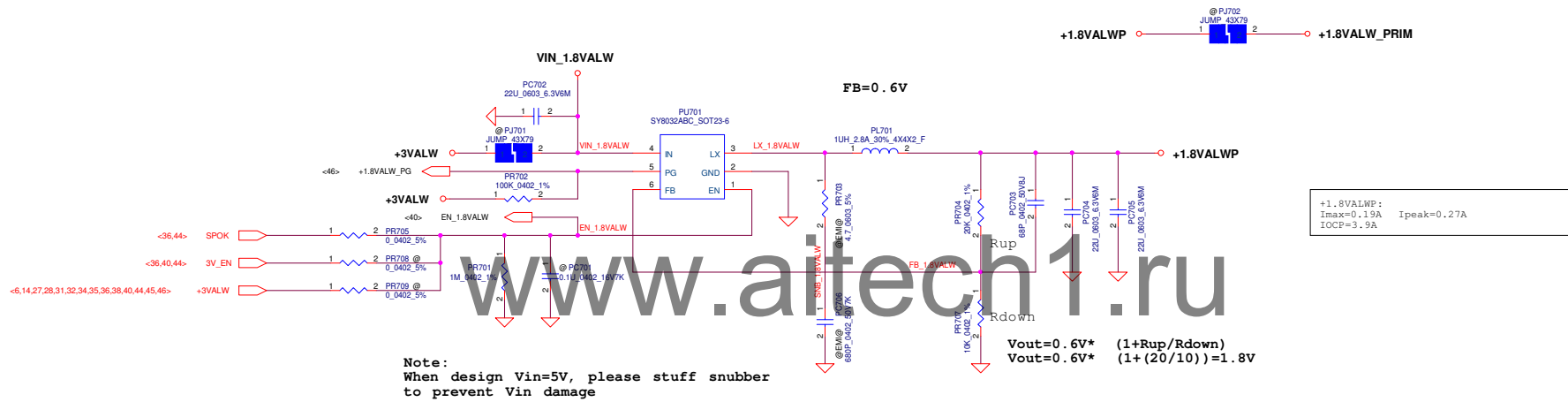
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				Date:	Friday, June 09, 2017	Sheet

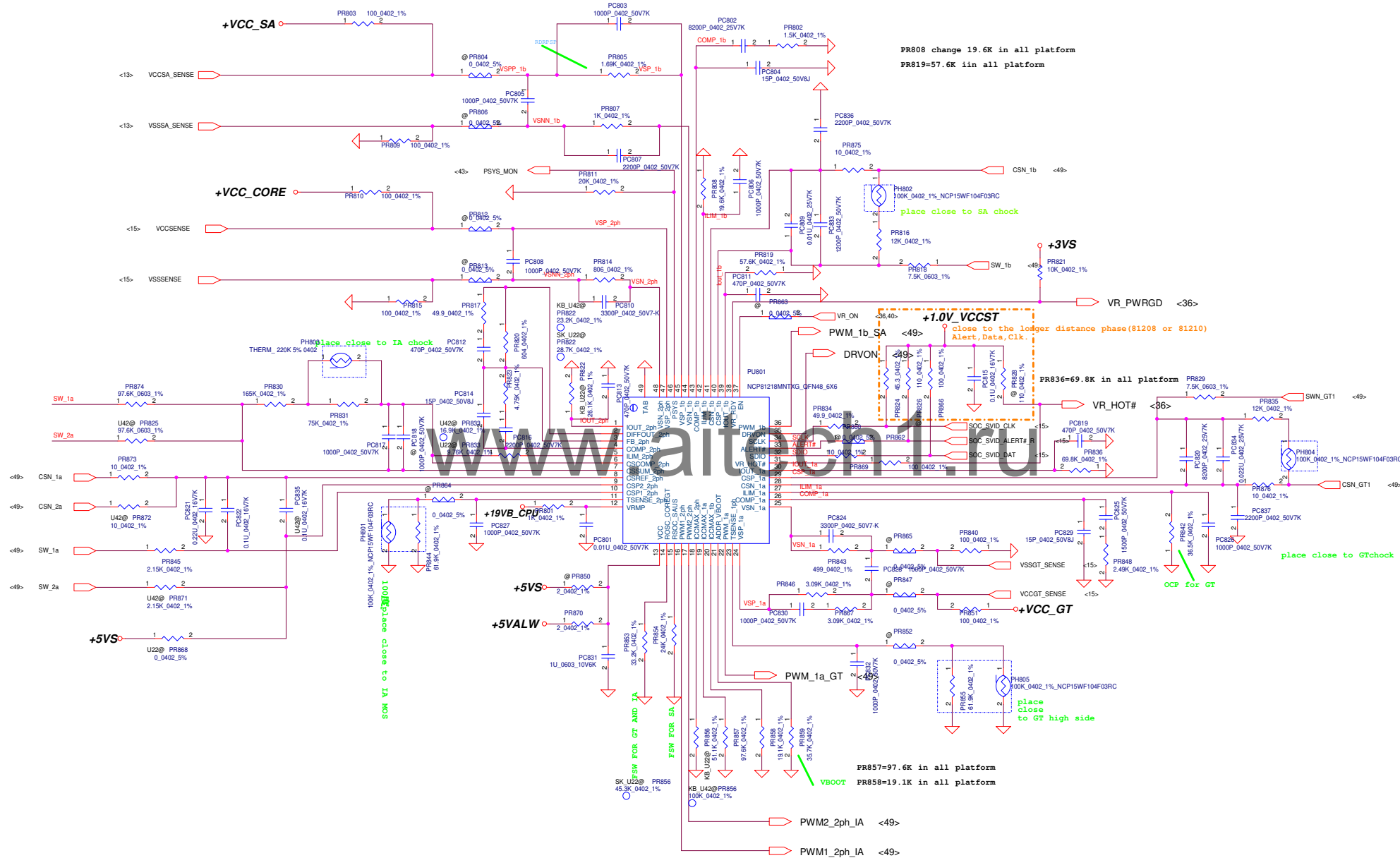


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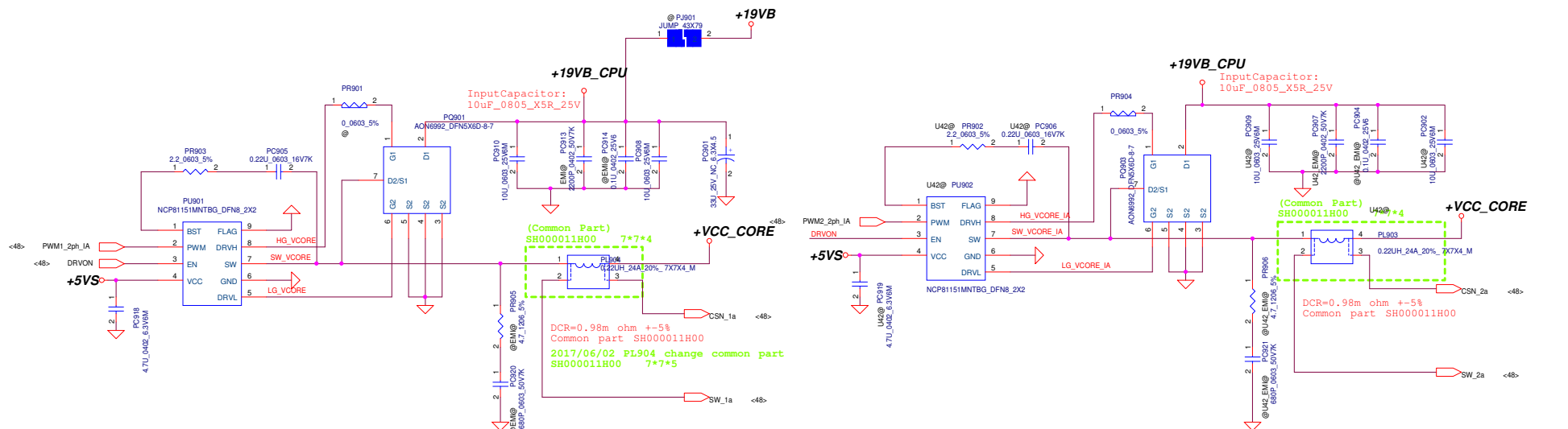
Module model information
SY8032_V2.mdd



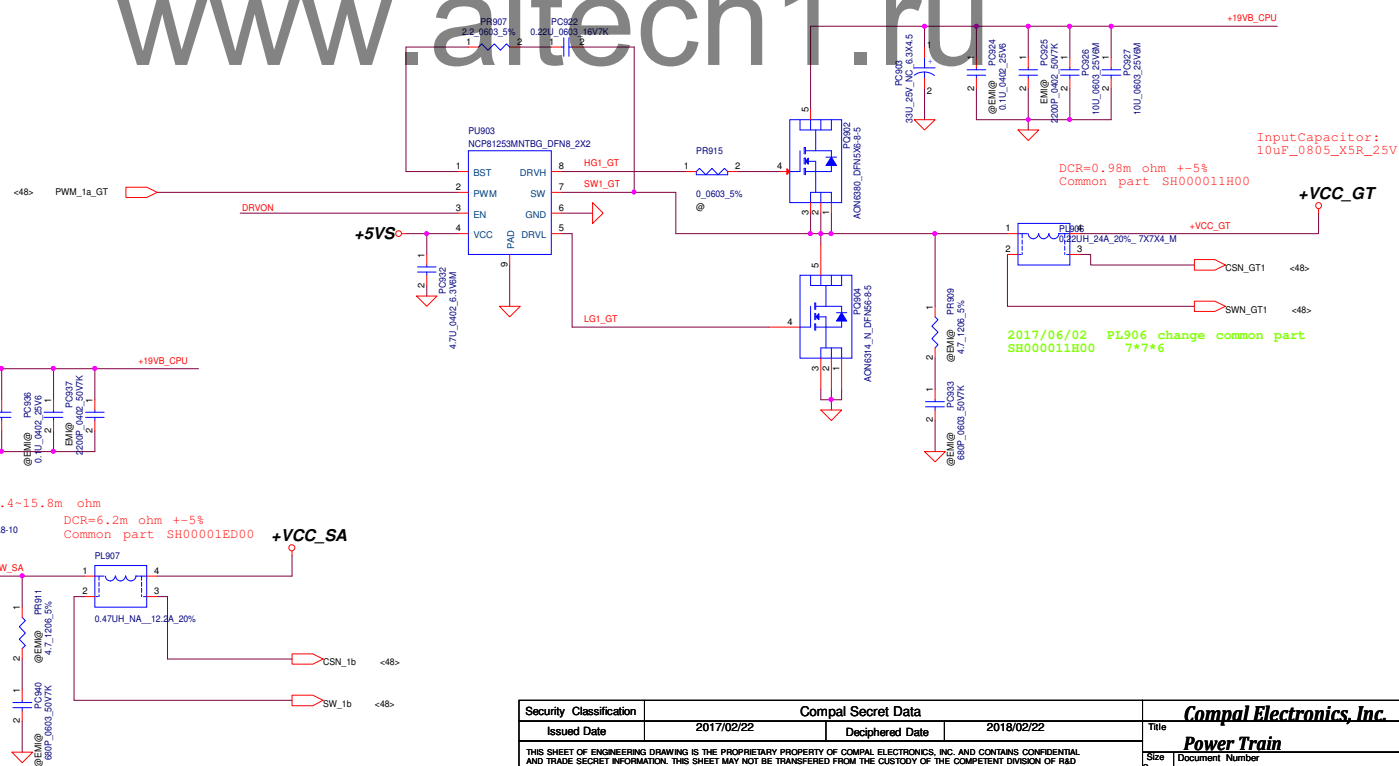


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				Size Document Number
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change PL9002, PL9003
SM01000C000 to comm
part SM01000P200



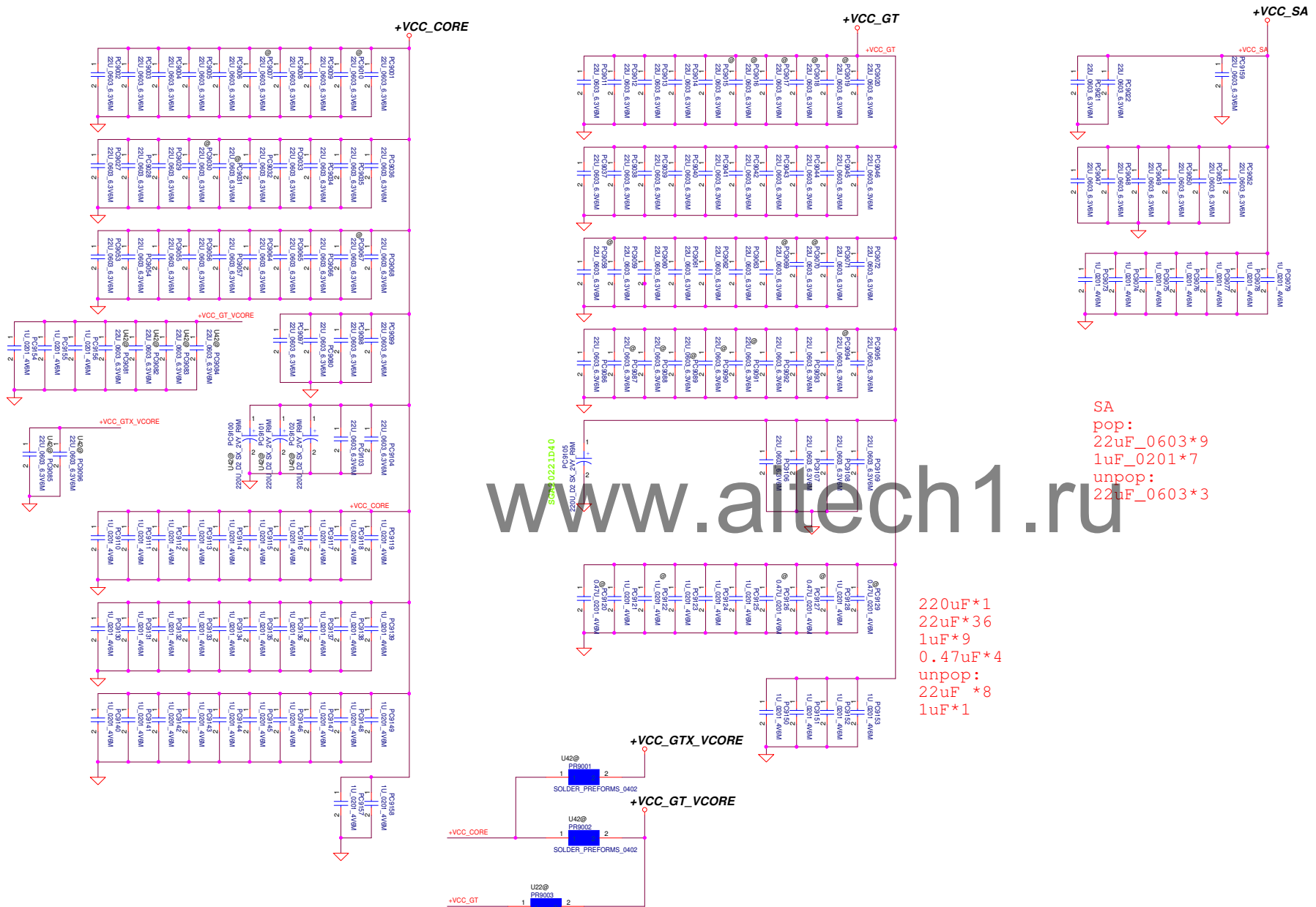
U22			
VCC:			
I _{max} =21A	I _{peak} =32A	I _{ocp} =40A	
U42			
VCC:			
I _{max} =42A	I _{peak} =64A	I _{ocp} =70A	
VCCGT:			
I _{max} =18A	I _{peak} =31A	I _{ocp} =39A	
VCCSA:			
I _{max} =4A	I _{peak} =5A	I _{ocp} =9.5A	



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2016/10/26
VCORE Output Capacitor:
U42
22uF_0603*39
1uF_0201*35
220uF *3
UNPOP
22_0603*3

2016/10/26
VCORE Output Capacitor:
U22
22uF_0603*33
1uF_0201*35
UNPOP
22_0603*9
220uF *3



220uF*1
22uF*36
1uF*9
0.47uF*4
unpop:
22uF *8
1uF*1

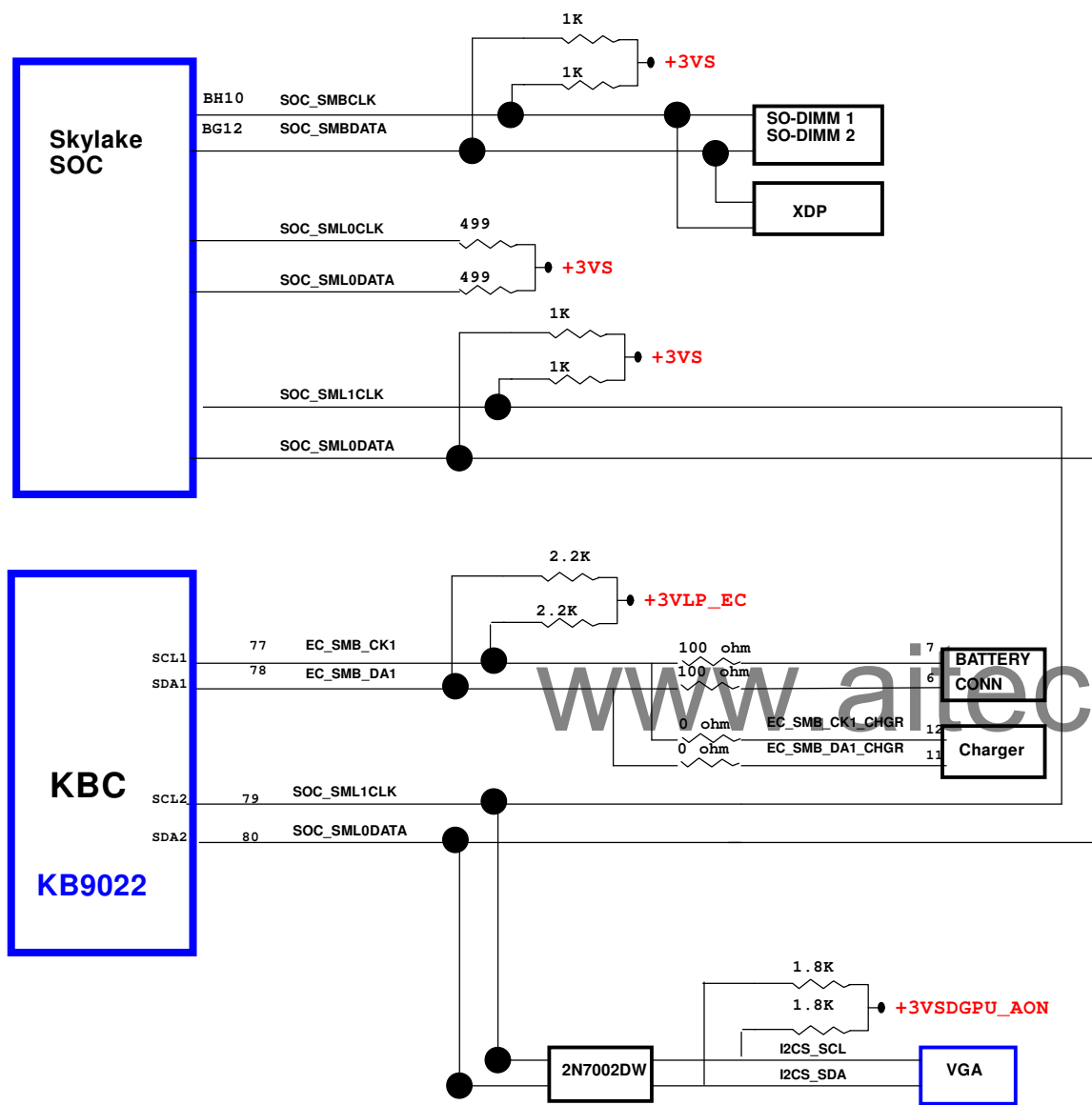
SA
pop:
22uF_0603*9
1uF_0201*7
unpop:
22uF_0603*3

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for PWR

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		C4PB1/C5PB1 LA-591			0.1
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P6->P6 U42
EVT_R0.1

4/24
1. ADD TS conn. JTS1
2. Add USB PORT 10 for TS function
3. Reserve USB PORT 6 test point(T3821,T3822) for NFC
4. Remove GPU circuit
5. Support PD charger in
6. ADD U5010 circuit for TS function
7. Add 24M XTAL(YC3) for KBL U42
8. +VCC_GTX_CORE contact to CPU (UC1.M)
9. +VCC_GT_CORE contact to CPU (UC1.M)
10. Add RC256
11. Del UC9 circuit
12. DEL RC58 (direct contact U11, U12)
13. Add TBTA_HV_GATE1/2 for PD in
14. Add TBTA_PD_SENSEP/N for PD in
15. DEL H23,H24
16. DEL RC204, RC195
17. Reserve test point T3812~3815 for GPU
18. update PARADE X76, X76525BOL05
19. Change RC38 to 121ohm
20. DEL XDP circuit
21. change RC182 to 0ohm@
22. Add R5274 for ME906
23. ADD HYNIX 8G SA0000ARA10 on board ram
24. ADD T3849
25. ADD SATAXPcie2
26. ADD R5276,R5275@, Q2023@ for PCIE SSD
27. Change Card reader to PCIE port4
28. ADD PCIE port 10 for PCIE_SSD
29. ADD CLK port 0 for PCIE_SSD
30. ADD D2018,D2019,D2020,D2021,D2022,D2023 for ESD
31. ADD CC435,CC436
32. ADD RC258

4/25
1. Q40,Q51,Q52,Q53,Q2006,Q2010,Q2013,Q2014,Q2016,
Q2017,Q2018,Q2019,Q2020,Q2021,QL2, change PN to SB000000SA00
2. Change U67 PN to SA00007IOA0 NPCT650ABCWX

4/26
Change U67 to SA00007IOA0

4/27
change R5207,R5208 to TBT@ and R5266,R5267 to @ for support dead battery

5/4
modify yellow BOM structure to meet white item
CC53,D17,D18,D19,D20,D21,D23,D24,R5196,R5204,R5207,R5208

PVT_R1.0

5/10
Swap JSSD1 PIN41,43 net

6/3
R401 chager to 47K for RF request(ME906)
Add RC 259 for CLKREQ_PCIE#0 pull up +3VS
change R5196,R4960 to @
change R5205 to 100Kohm TBT@
change R659 to mount
change UC2 PN to SA00005VV20
swap JSSD PCIE port 11,12
SSD_DET# connect to SATAXPcie1
change R4903 to 12K
Add C5265 for PCIE SSD power
Add Adp_det
change R4938 to 0ohm
VCOUt1_PROCHOT connect to HPROCHOT#
remove J13 for C5265

6/8
Add R5277 for +5VS_CRT_SW
Add L4905 for +3VS_CRT_SW
SW_PROCHOT# connect to H_PROCHOT#
Change R4960 to mount
Change R523,R4938,R5276 to short pad
Change R5260 to 0ohm
Add Q2024,R5279,R5278 for +1.8VALW_PRIM discharge circuit
Change UU24, CU181, RU165 to @

6/8A
remove RC151

6/9
change R5193 to 0ohm_0402

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				Size	Document Number		Rev 1.0
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DDR4 On Board RAM

X76713BOL03 Hynix	X76713BOL01 micron 4G	X76713BOL02 micron 8G	X76713BOL06 HYNIX 8G
<div><div>U2</div><div>D4 512M16 H5AN8G6NAFR SA0000A1H20</div><div>X76OBHY@</div></div> <div><div>U3</div><div>D4 512M16 H5AN8G6NAFR SA0000A1H20</div><div>X76OBHY@</div></div> <div><div>U4</div><div>D4 512M16 H5AN8G6NAFR SA0000A1H20</div><div>X76OBHY@</div></div> <div><div>U5</div><div>D4 512M16 H5AN8G6NAFR SA0000A1H20</div><div>X76OBHY@</div></div>	<div><div>U2</div><div>D4 512M16 MT40A512M16JY SA00009V220</div><div>X76OBMACRON4@</div></div> <div><div>U3</div><div>D4 512M16 MT40A512M16JY SA00009V220</div><div>X76OBMACRON4@</div></div> <div><div>U4</div><div>D4 512M16 MT40A512M16JY SA00009V220</div><div>X76OBMACRON4@</div></div> <div><div>U5</div><div>D4 512M16 MT40A512M16JY SA00009V220</div><div>X76OBMACRON4@</div></div>	<div><div>U2</div><div>D4 16G MT40A1G16WBU SA0000A3120</div><div>X76OBMACRON8@</div></div> <div><div>U3</div><div>D4 16G MT40A1G16WBU SA0000A3120</div><div>X76OBMACRON8@</div></div> <div><div>U4</div><div>D4 16G MT40A1G16WBU SA0000A3120</div><div>X76OBMACRON8@</div></div> <div><div>U5</div><div>D4 16G MT40A1G16WBU SA0000A3120</div><div>X76OBMACRON8@</div></div>	<div><div>U2</div><div>D4 16G/2400 H5ANAG6NAMR SA0000ARA10</div><div>X76OBHYNIX8@</div></div> <div><div>U3</div><div>D4 16G/2400 H5ANAG6NAMR SA0000ARA10</div><div>X76OBHYNIX8@</div></div> <div><div>U4</div><div>D4 16G/2400 H5ANAG6NAMR SA0000ARA10</div><div>X76OBHYNIX8@</div></div> <div><div>U5</div><div>D4 16G/2400 H5ANAG6NAMR SA0000ARA10</div><div>X76OBHYNIX8@</div></div>

VRAM

X76614BOL54 Hynix	X76614BOL58 SANSUNG	X76713BOL04 Hynix E-die
<div><div>U2004</div><div>D3 256M16 H5TC4G63CFR SA00008DN10</div><div>X76VHY@</div></div> <div><div>U2005</div><div>D3 256M16 H5TC4G63CFR SA00008DN10</div><div>X76VHY@</div></div> <div><div>U2006</div><div>D3 256M16 H5TC4G63CFR SA00008DN10</div><div>X76VHY@</div></div> <div><div>U2007</div><div>D3 256M16 H5TC4G63CFR SA00008DN10</div><div>X76VHY@</div></div>	<div><div>U2004</div><div>D3 256M16 K4W4G1646E SA000076PB0</div><div>X76VSAM@</div></div> <div><div>U2005</div><div>D3 256M16 K4W4G1646E SA000076PB0</div><div>X76VSAM@</div></div> <div><div>U2006</div><div>D3 256M16 K4W4G1646E SA000076PB0</div><div>X76VSAM@</div></div> <div><div>U2007</div><div>D3 256M16 K4W4G1646E SA000076PB0</div><div>X76VSAM@</div></div>	<div><div>U2004</div><div>S IC D3 256M16 H5TC4G63EFR-N0C SA00008DN80</div><div>X76VHY_E@</div></div> <div><div>U2005</div><div>S IC D3 256M16 H5TC4G63EFR-N0C SA00008DN80</div><div>X76VHY_E@</div></div> <div><div>U2006</div><div>S IC D3 256M16 H5TC4G63EFR-N0C SA00008DN80</div><div>X76VHY_E@</div></div> <div><div>U2007</div><div>S IC D3 256M16 H5TC4G63EFR-N0C SA00008DN80</div><div>X76VHY_E@</div></div>

SATA Redriver

X76525BOL51 TI	X76713BOL05 Parade	X76525BOL52 Parade
<div><div>U1</div><div>SN75LVCP601RTJR SA00003ZX00</div><div>X76SATATi@</div></div> <div><div>R11</div><div>4.99K +-1% 0402 SD034499180</div><div>X76SATATi@</div></div>	<div><div>U1</div><div>PS8527CTQFN20GTR2-A2 SA00007JU10</div><div>X76SATAPAR@</div></div> <div><div>R18</div><div>4.7K +-5% 0402 SD028470180</div><div>X76SATAPAR@</div></div> <div><div>R11</div><div>7.5K +-5% 0402 SD028100280</div><div>X76SATAPAR@</div></div>	<div><div>U1</div><div>PS8527CTQFN20GTR2-A1 SA00007JU00</div><div>X76SATAPARa@</div></div> <div><div>R18</div><div>4.7K +-5% 0402 SD028470180</div><div>X76SATAPARa@</div></div> <div><div>R11</div><div>7.5K +-5% 0402 SD028100280</div><div>X76SATAPARa@</div></div>

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